Schematic Package Supplement to

DRAGON'S LAIR*

Operators Manual

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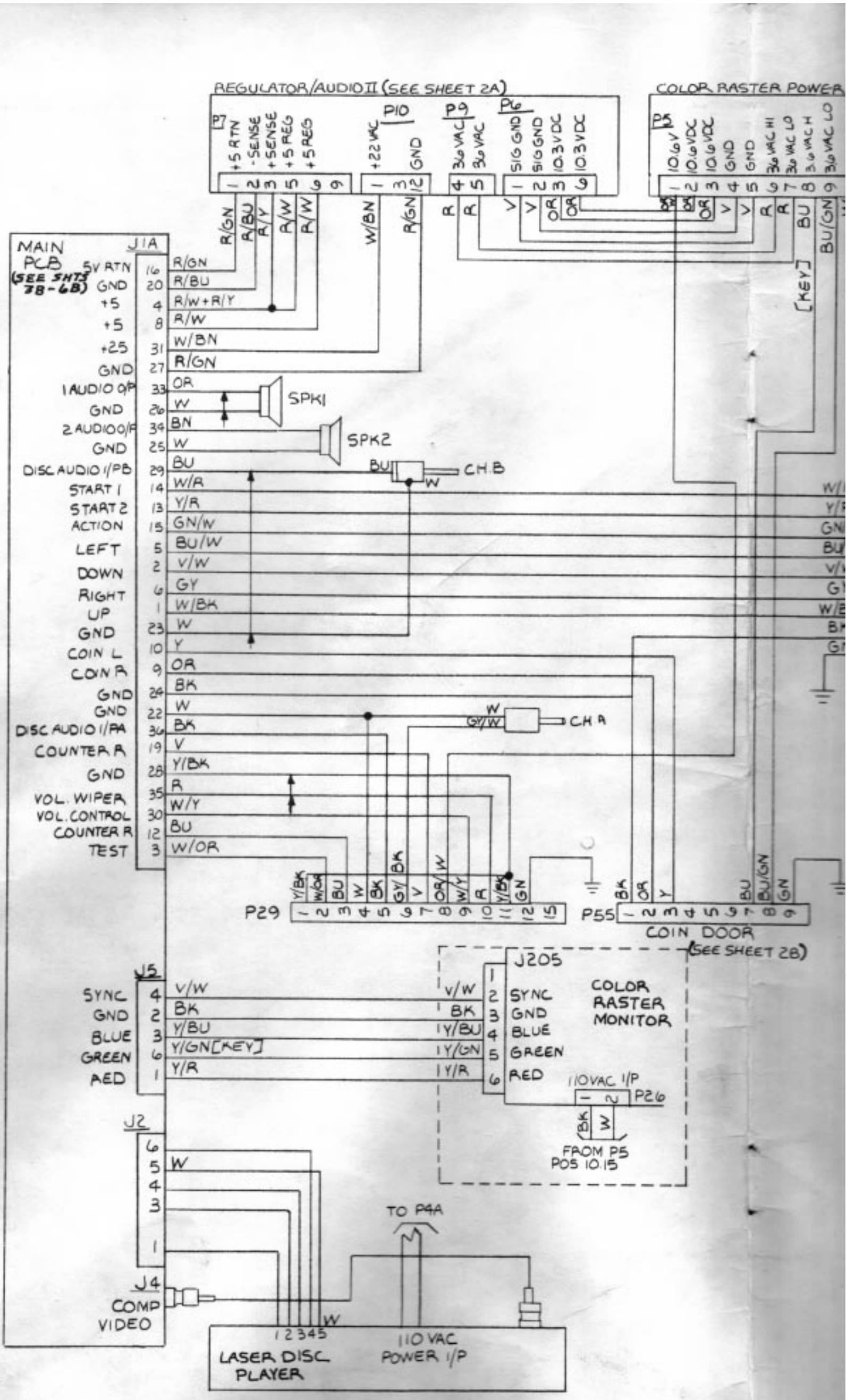
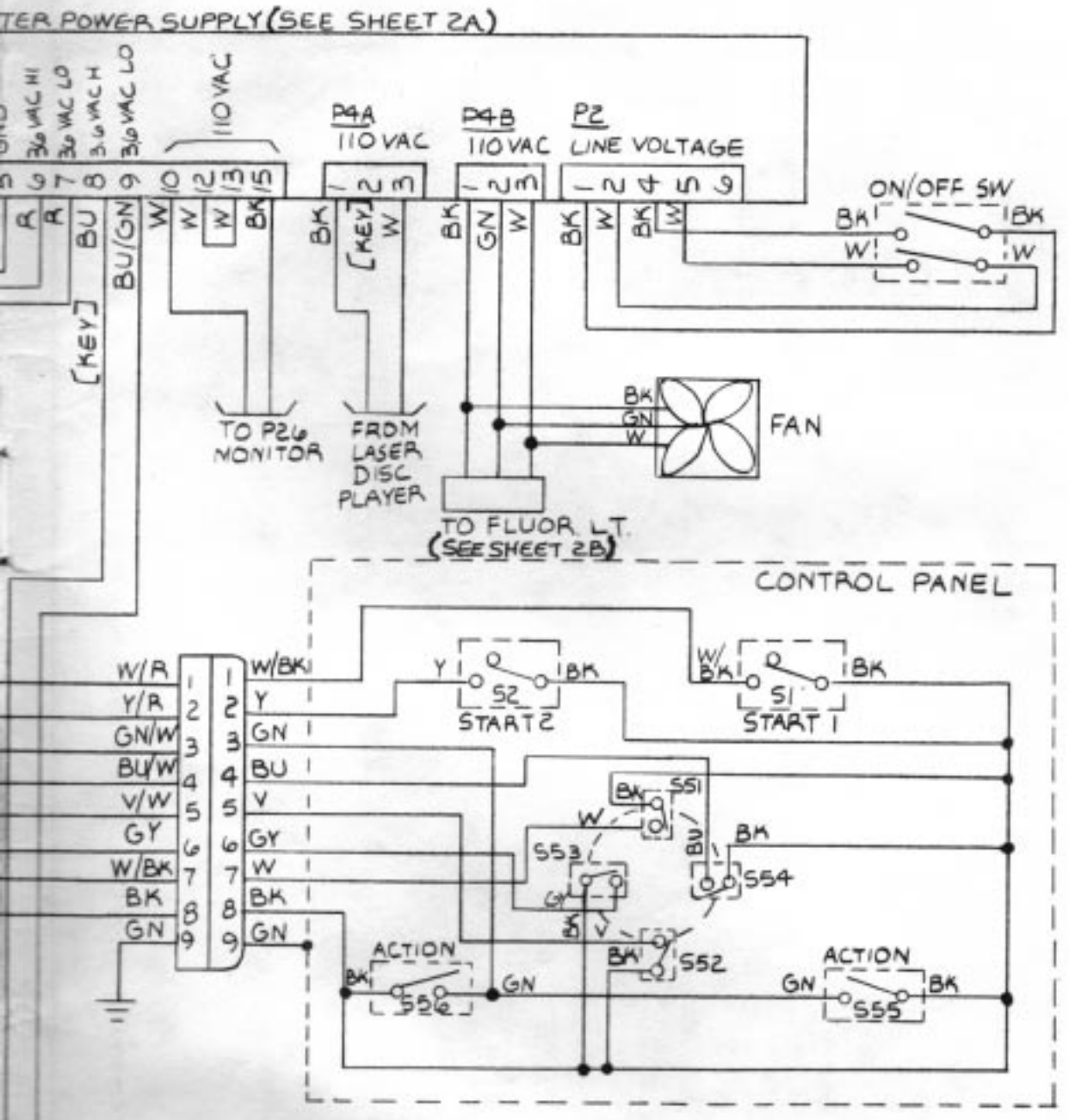
NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

Table of Contents


REGULATOR/AUDIO II (SEE SHEET 2A)
P7
+5 RTN
-SENSE
+SENSE
+5 REG
+5 REG
P10
+22 VAC
GND
P9
36 VAC
36 VAC
P6
SIG GND
SIG GND
10.3 VDC
10.3 VDC
COLOR RASTER POWER
10.6 V
10.6 VDC
10.6 VDC
GND
GND
36 VAC HI
36 VAC LO
36 VAC H
36 VAC LO
[KEY]
MAIN PCB (SEE SHTS 7B-6B)
J1A
5V RTN 16
GND 20
+5 4
+5 8
+25 31
GND 27
1 AUDIO O/P 33
GND 26
2 AUDIO O/P 34
GND 25
DISC AUDIO 1/PB 29
START 1 14
START 2 13
ACTION 15
LEFT 5
DOWN 2
RIGHT 6
UP 1
GND 23
COIN L 10
COIN R 9
GND 24
GND 22
DISC AUDIO 1/PA 36
COUNTER A 19
GND 28
VOL. WIPER 35
VOL. CONTROL 30
COUNTER B 12
TEST 3
R/GN
R/BU
R/W+R/Y
R/W
W/BN
R/GN
OR
W
BN
W
BU
W/R
Y/R
GN/W
BU/W
V/W
GY
W/BK
W
Y
OR
BK
W
BK
V
Y/BK
R
W/Y
BU
W/OR
SPK1
SPK2
BU
W
CH B
W
GY/W
CH A
P29
Y/BK
W/OR
BU
W
BK
GY/BK
V
OR/W
W/Y
R
Y/BK
GN
P55
BK
OR
Y
BU
BU/GN
GN
COIN DOOR
(SEE SHEET 2B)
J5
SYNC 4
GND 2
BLUE 3
GREEN 6
RED 1
V/W
BK
Y/BU
Y/GN[KEY]
Y/R
J205
COLOR RASTER MONITOR
1
2 SYNC
3 GND
4 BLUE
5 GREEN
6 RED
110VAC I/P
P26
BK
W
FROM P5 POS 10.15
J2
6
5 W
4
3
1
J4
COMP VIDEO
TO P4A
1 2 3 4 5
W
LASER DISC PLAYER
110 VAC POWER I/P



Dragon's Lair Main Wiring Diagram

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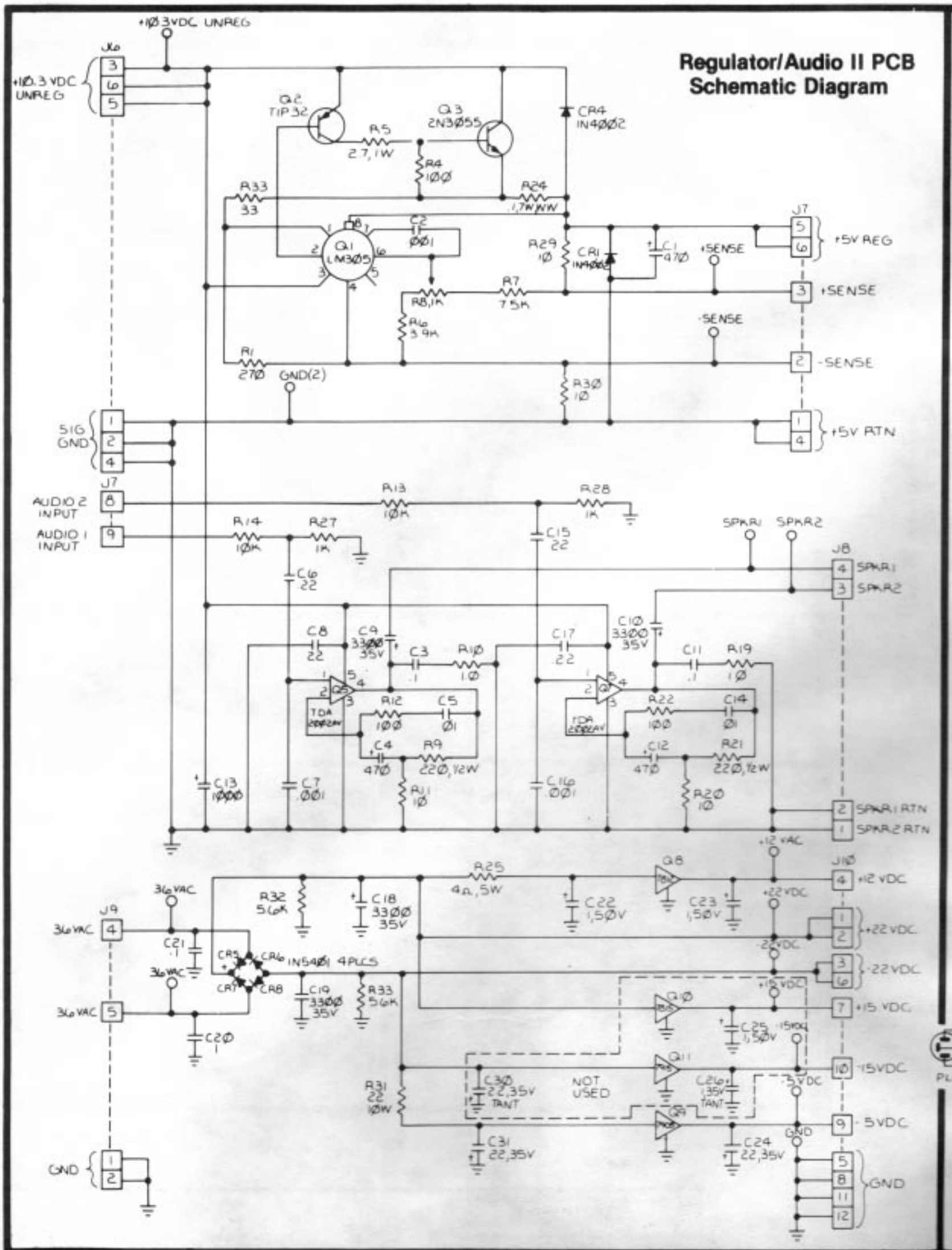
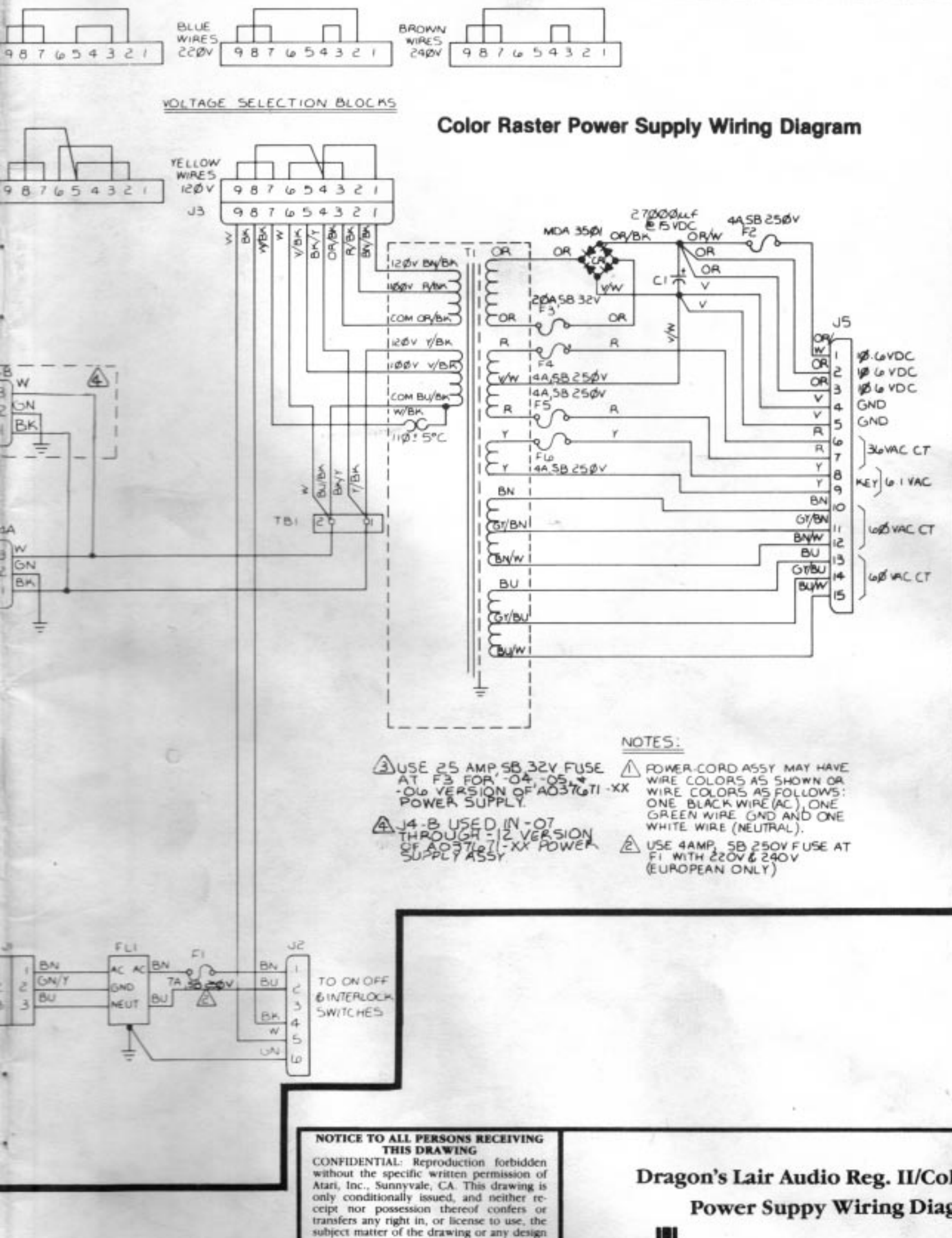
Regulator/Audio II PCB Schematic Diagram



Color Raster Power Supply Wiring Diagram



NOTES:

3. USE 25 AMP, SB 32V FUSE AT F3 FOR -04, -05, -06 VERSION OF A037607I-XX POWER SUPPLY.
4. J4-B USED IN -07 THROUGH -12 VERSION OF A037607I-XX POWER SUPPLY ASSY.
1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE GND AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)

Dragon's Lair Audio Reg. II/Color Raster Power Suppy Wiring Diagram

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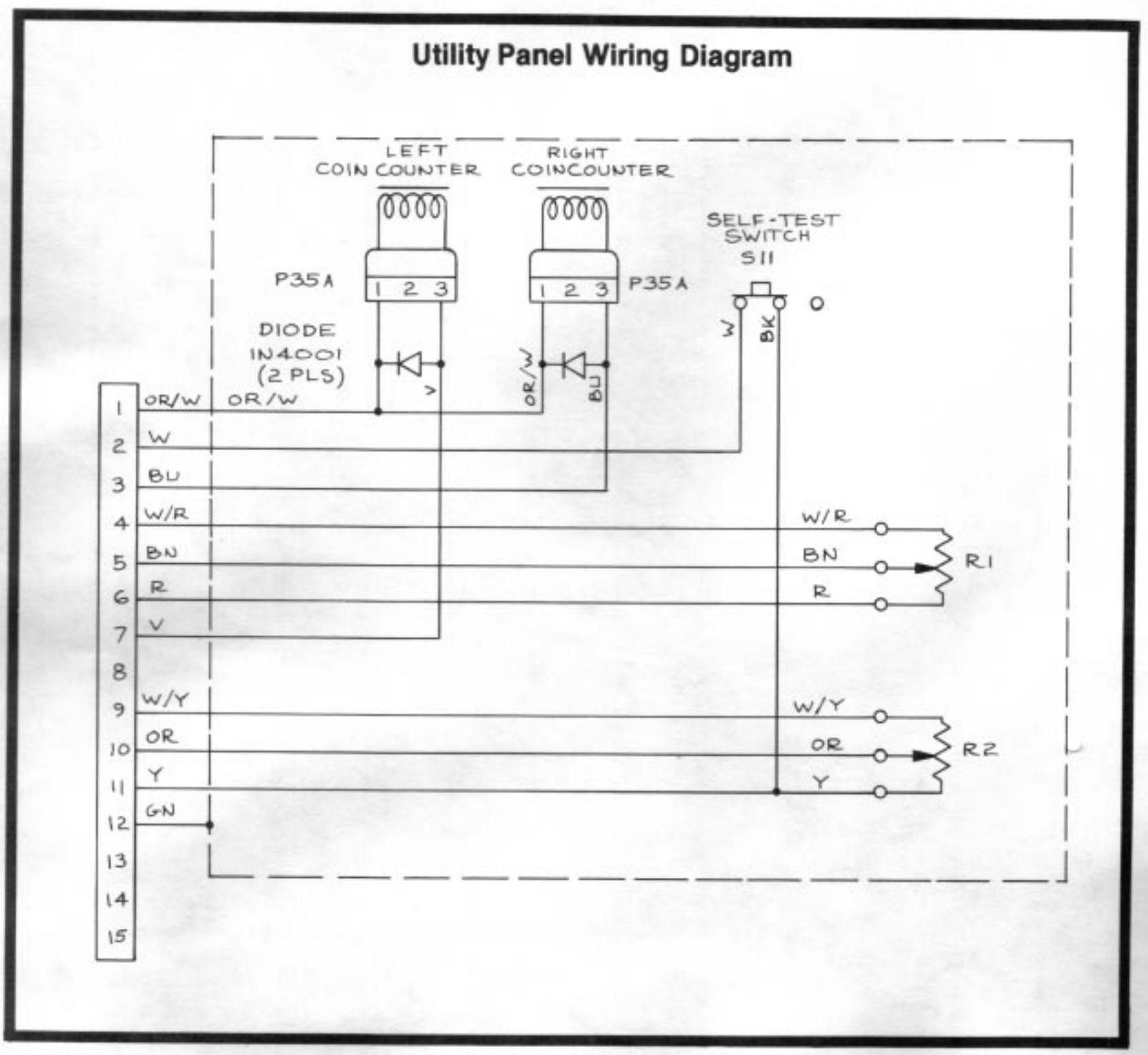
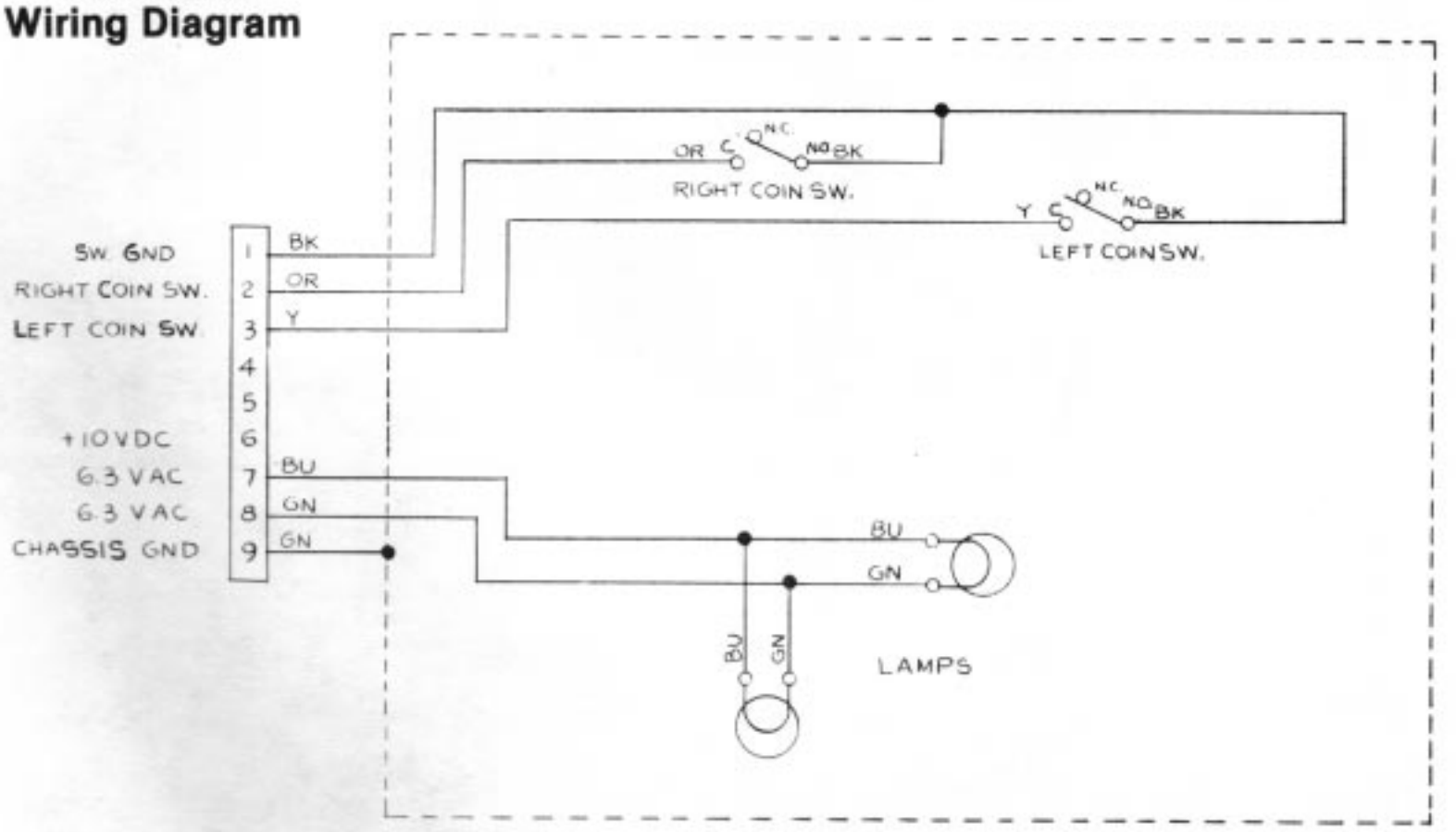
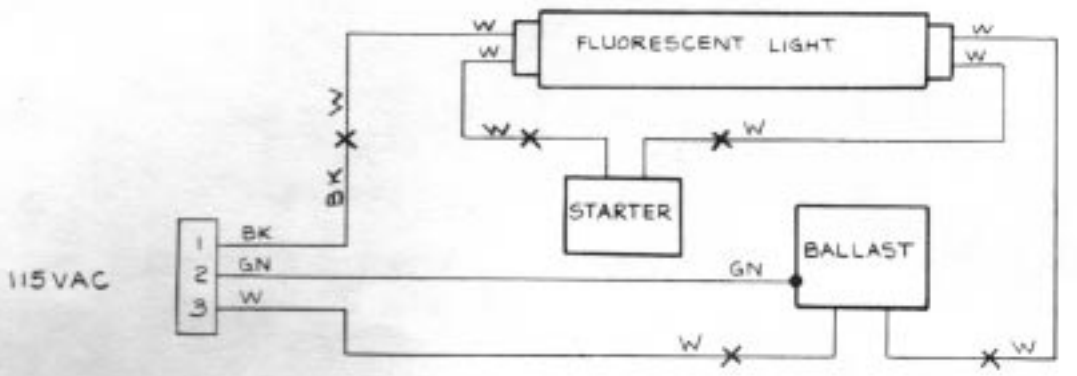
Utility Panel Wiring Diagram



Coin Door Wiring Diagram



Fluorescent Light Wiring Diagram



Dragon's Lair Game Interfaces

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Memory Request

NOTE

The CAT Box/Z80 Interface jumper plug must be connected to J1 to check the address and data lines in the following memory map.

HEXA-DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	READ/ WRITE	DATA BUS SIGNAL LINES D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0008	0	0	0		0	0	0	0	0		0	0					W									Watchdog Reset
0010	0	0	0						0		0	1	0				W								D	Character Gen. Enable
																	W							D		Kill Video
																	W						D			Character Gen./Disc Video Select
																	W					D				Coin Counter 2
																	W				D					Coin Counter 1
																	W	D	D	D						Not Used
0030	0	0	0						0		1	1	0				W	D	D	D	D	D	D	D	D	LED 2 Display
0038	0	0	0						0		1	1	1				W	D	D	D	D	D	D	D	D	LED 1 Display
00A0	0	0	0						1		1	0	0				R	D								Not Used
00A0	0	0	0						1		1	0	0				R		D	D	D	D	D	D	D	Option Switch B
00A8	0	0	0						1		1	0	1				R	D	D	D	D	D	D	D	D	Option Switch A
00B0	0	0	0						1		1	1	0				R								D	Start 1 Switch
																	R							D		Start 2 Switch
																	R						D			Coin 1 Switch
																	R					D				Coin 2 Switch
																	R				D					Not Used
																	R			D						Not Used
																	R		D							Not Used
																	R	D								Not Used
00B8	0	0	0						1		1	1	1				R								D	Joystick Up
																	R							D		Joystick Down
																	R						D			Joystick Left
																	R					D				Joystick Right
																	R				D					Action
																	R			D						Not Used
																	R		D							Not Used
																	R	D								Self-Test
2000–27FF	0	0	1			A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	Character Gen. RAM
4000–47FF	0	1	0			A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	Working RAM
6000–7FFF	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM4
8000–9FFF	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM3
A000–BFFF	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM2
C000–DFFF	1	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM1
E000–FFFF	1	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM0

Input/Output Request

NOTE

The CAT Box/Z80 Interface jumper plug must be connected to J2 to check the address and data lines in the following memory map.

HEXA-DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	READ/ WRITE	DATA BUS SIGNAL LINES D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0080–0085									1						A	A	R/W	D	D	D	D	D	D	D	D	DART
0003									0						1	1	R/W	D	D	D	D	D	D	D	D	CTC

Dragon's Lair Memory Map

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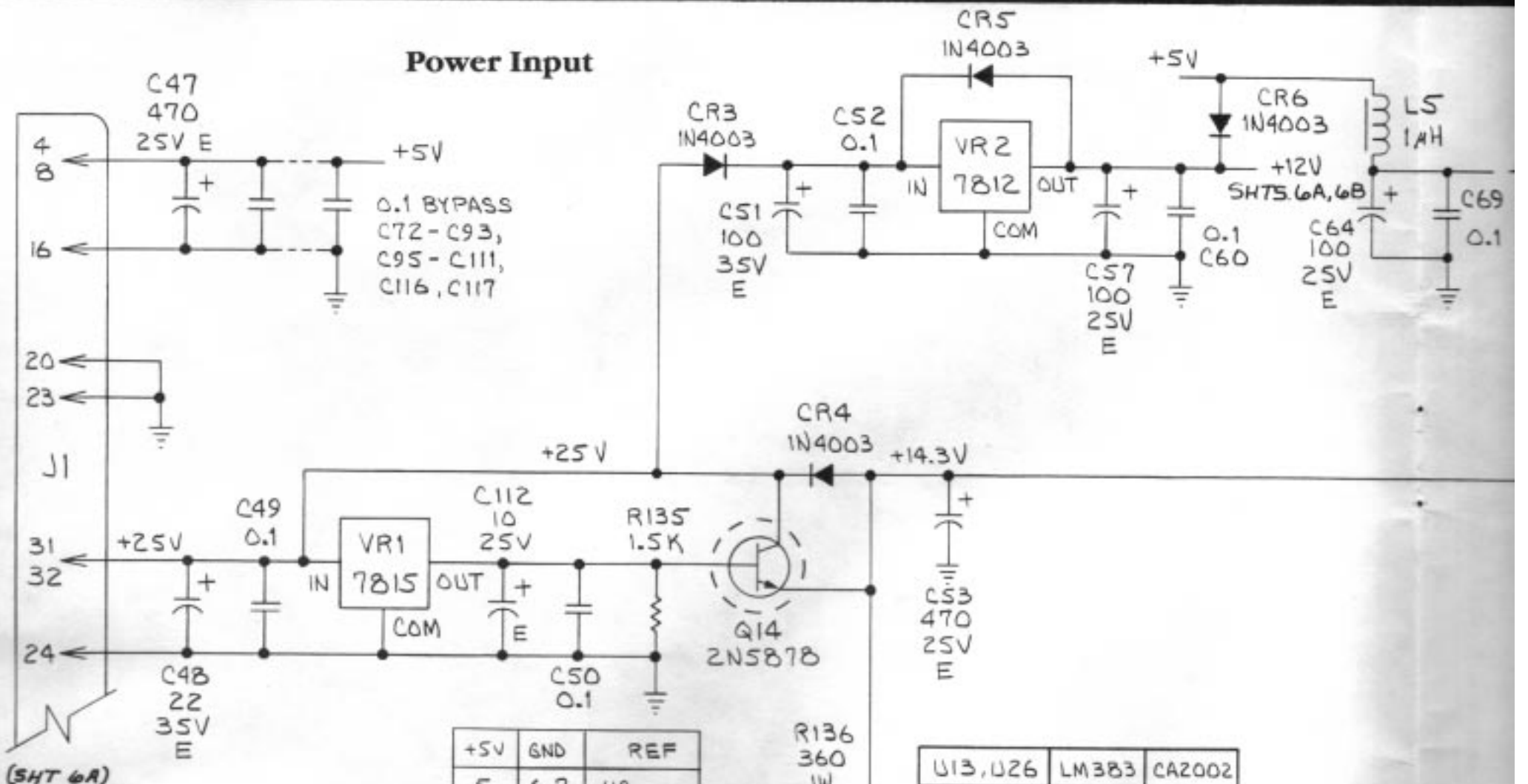
Power Input



4. POWER DISTRIBUTION

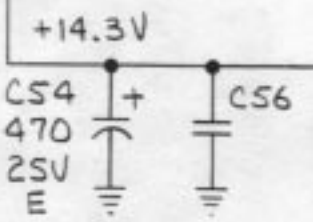
+5V	GND	IC REFERENCE
14	7	U1-5, 10-12, 15-18, 20-25, 60, 66
16	8	U8, 34, 59, 63, 64
20	10	U19, 28, 30, 31, 35-37, 40-43, 50-58, 62, 65
24	12	U6, 7, 32, 28, 69
28	14	U33, 45-49

+5V	GND	REF
5	6,7	U9
9	31	U27
11	29	U29
25	4	U14

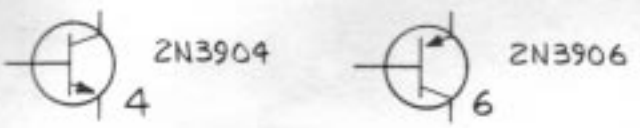
+12V	GND	REF
1	27	U61
4,8	1	U67, 68
14	7	U44

+14.3V	GND	REF
5	3	U13, 26

U13, U26	LM383	CA2002
R142, R144	0Ω	2.2Ω
C55, C56, C66, C68	0.2	0.1



3. TRANSISTORS



2. CAPACITOR VALUES ARE IN MICRO FARADS
   CAPACITORS ARE CERAMIC DISC, 50 V
   E SIGNIFIES ELECTROLYTIC CAPACITOR
   LLE SIGNIFIES LOW LEAKAGE ELECTROLYTIC CAPACITOR
   F SIGNFIES FILM CAPACITOR

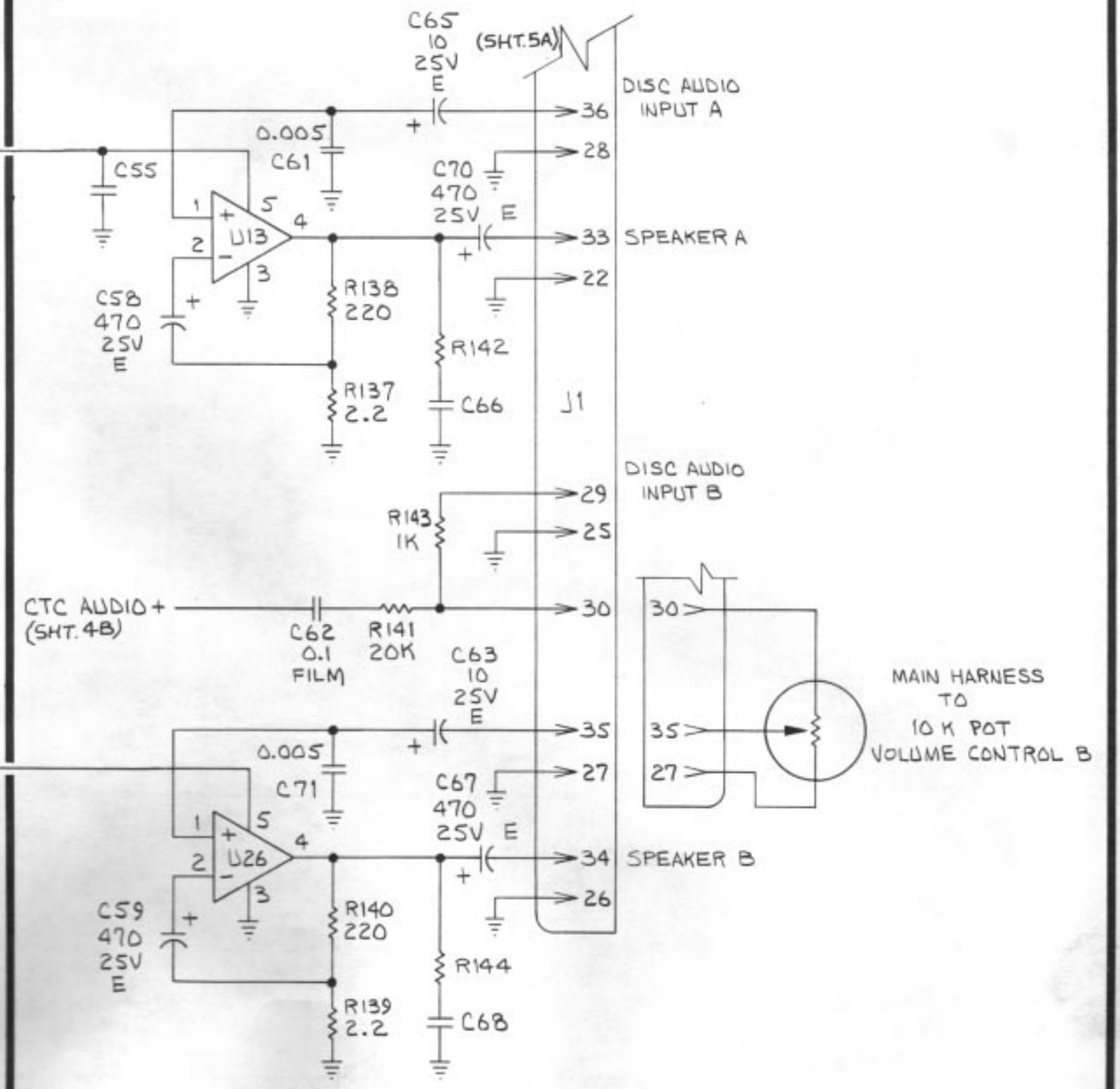
1. RESISTOR VALUES ARE IN OHMS; RESISTORS ARE 1/4W 5% CARBON

LS
1μH

+5V F

C69 (SHT. 6A)
0.1

Audio Amp/Output



Dragon's Lair Main PCB
Schematic Diagram

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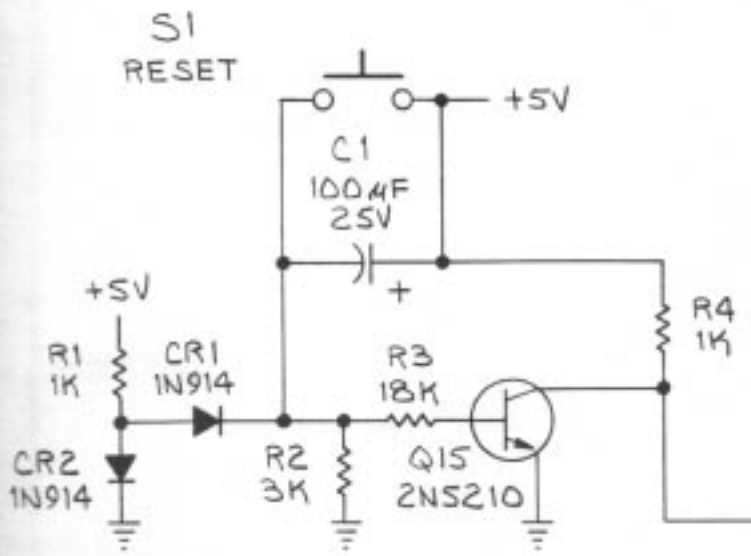
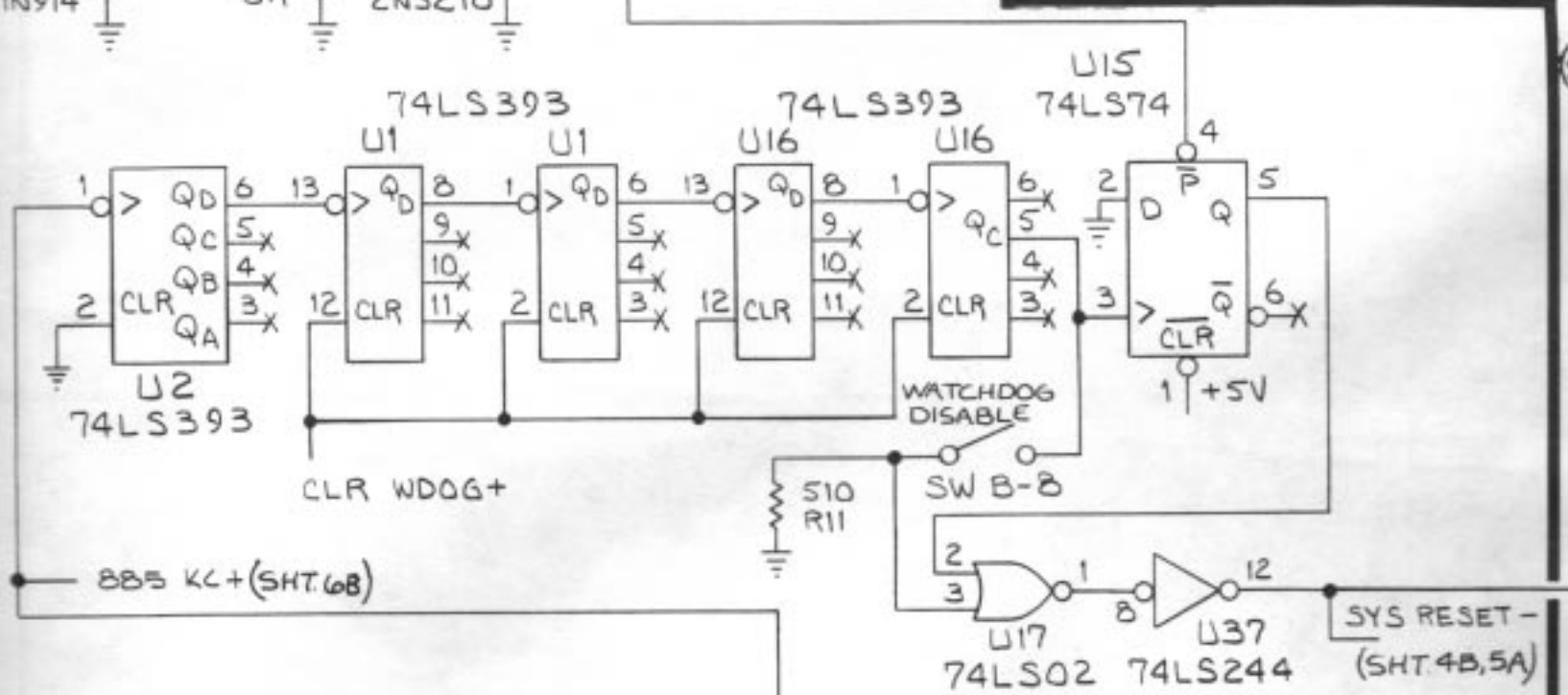
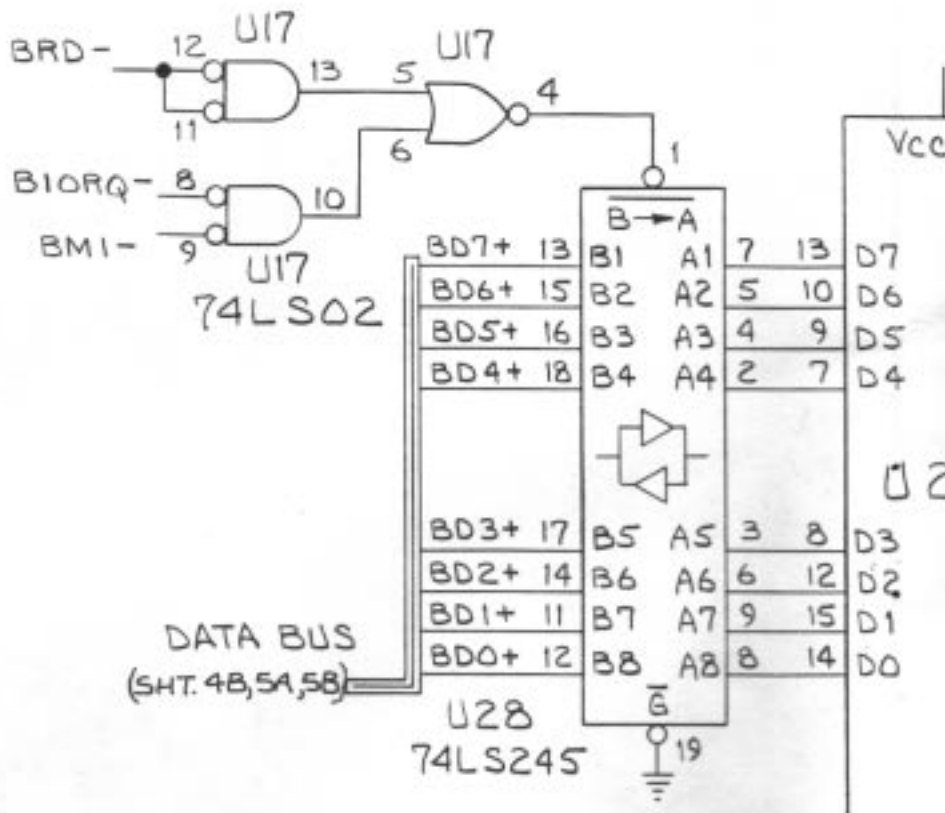
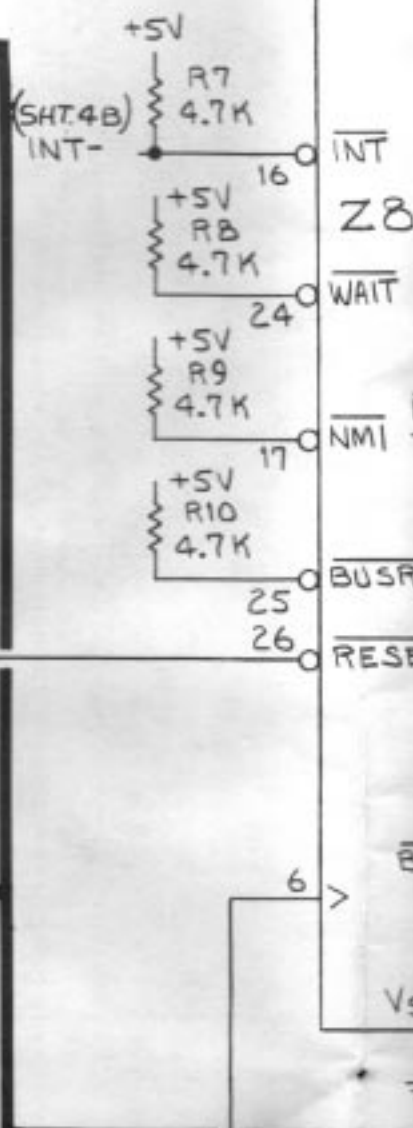
Watchdog and Reset

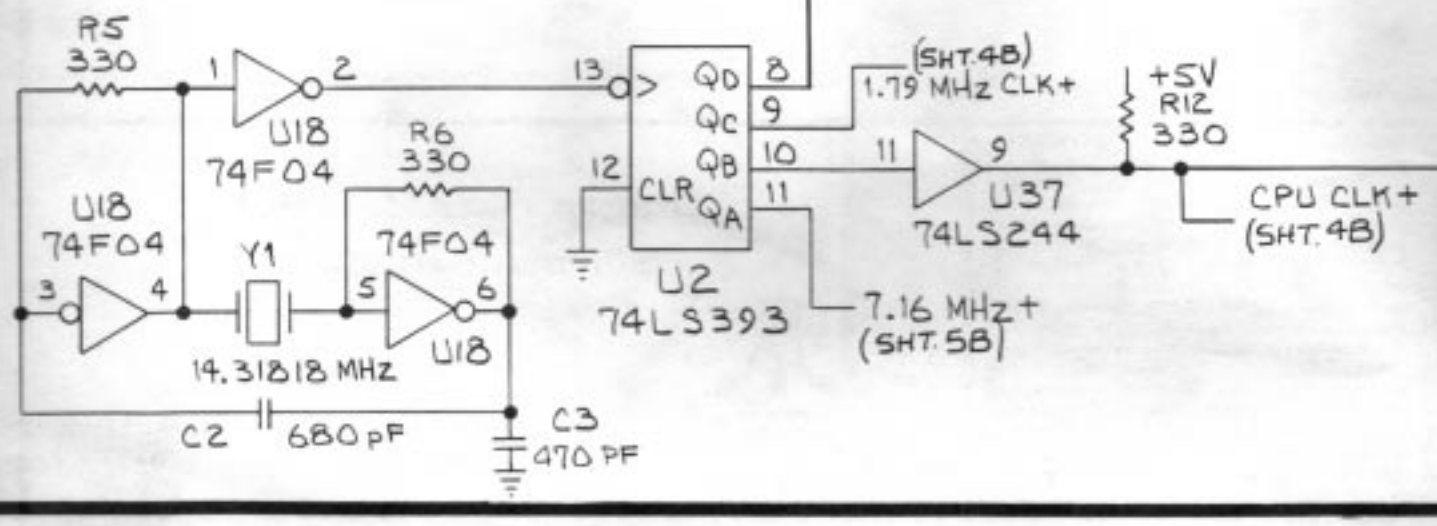








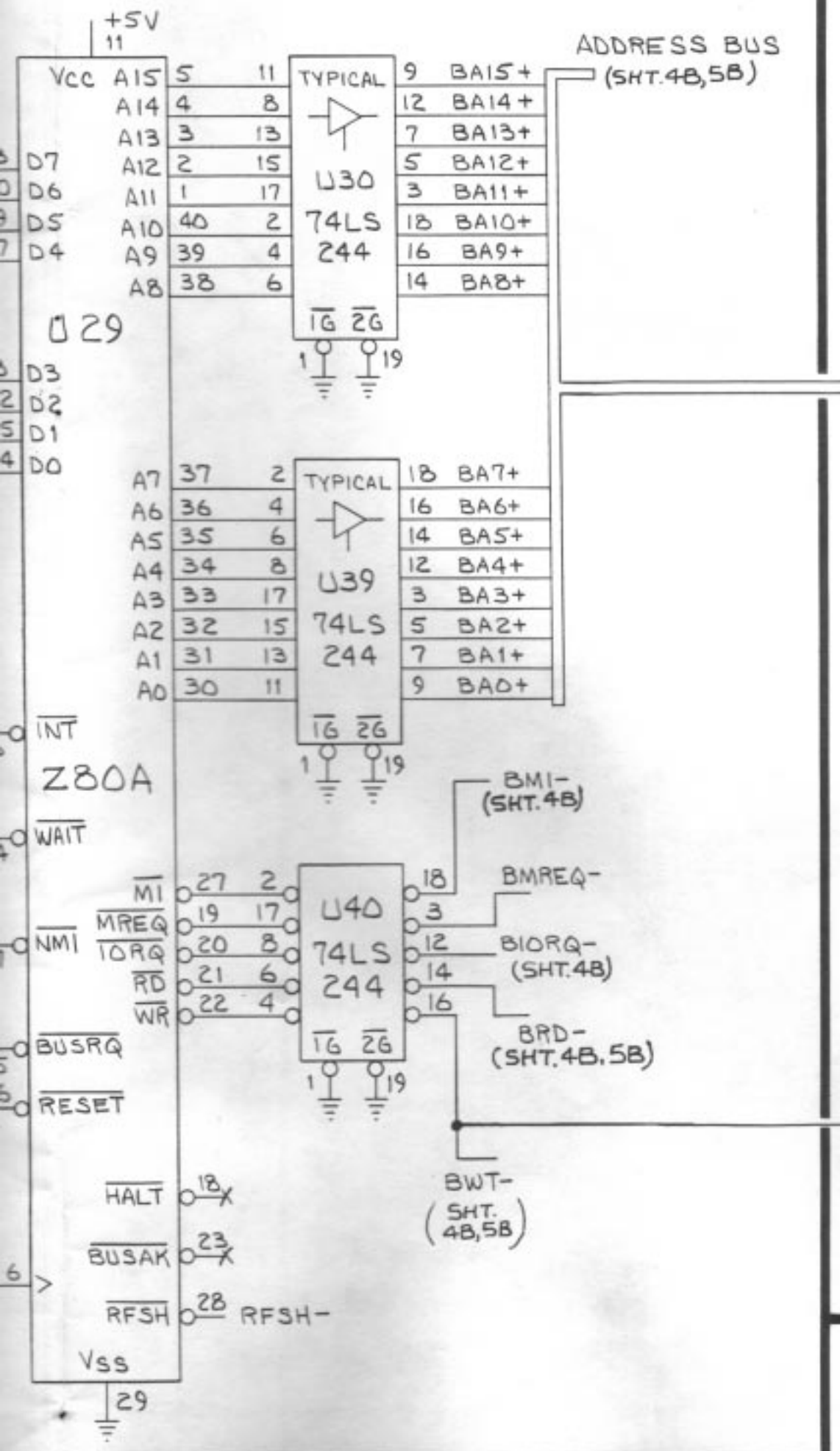
Microprocessor Clock



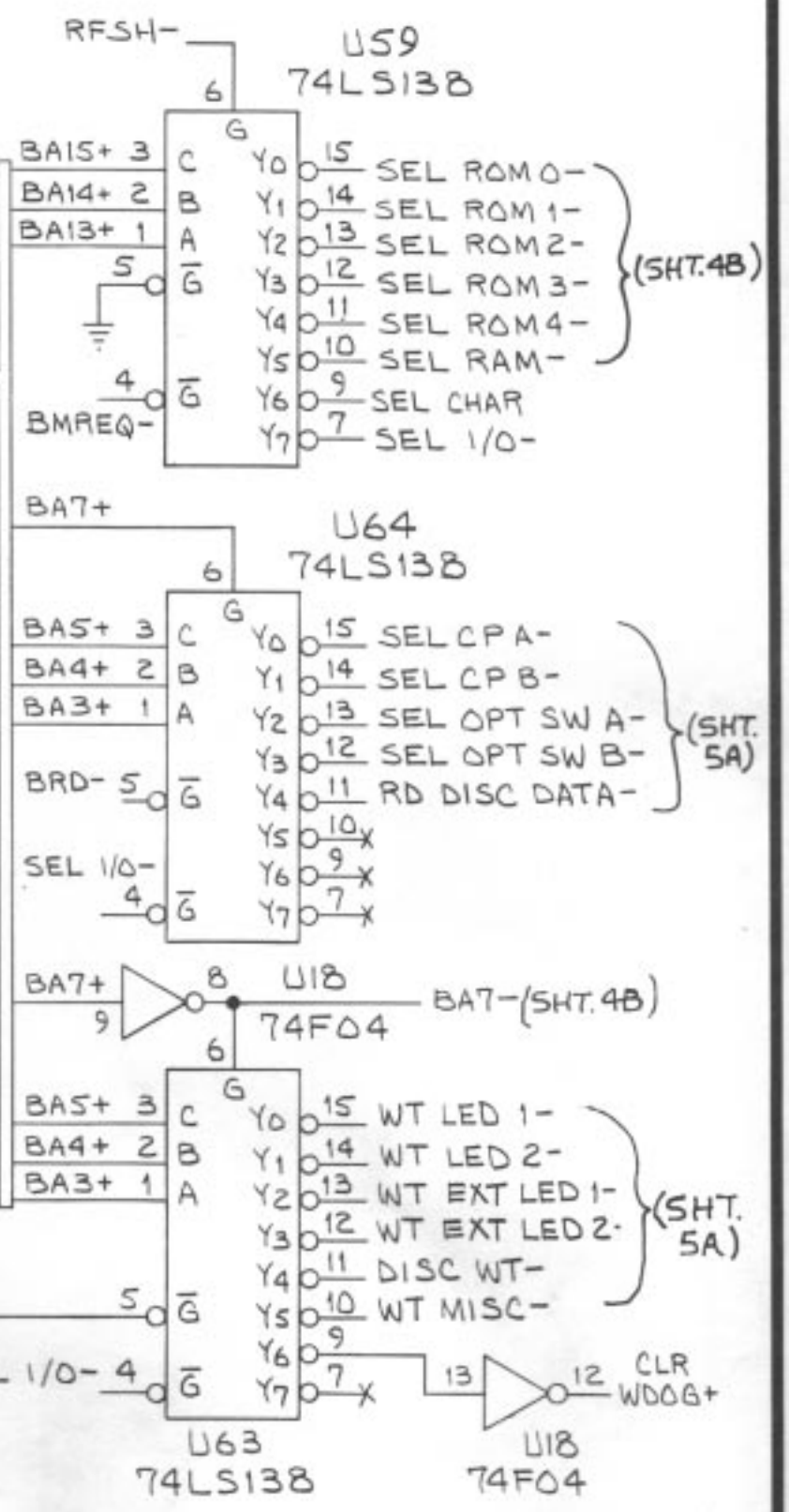
NO

Plus (+) after a
dicates active h
after a signal lin
tive low.

Microprocessor



Address Decoder



NOTE

Plus (+) after a signal line indicates active high. Minus (−) after a signal line indicates active low.

Dragon's Lair Main PCB
Schematic Diagram

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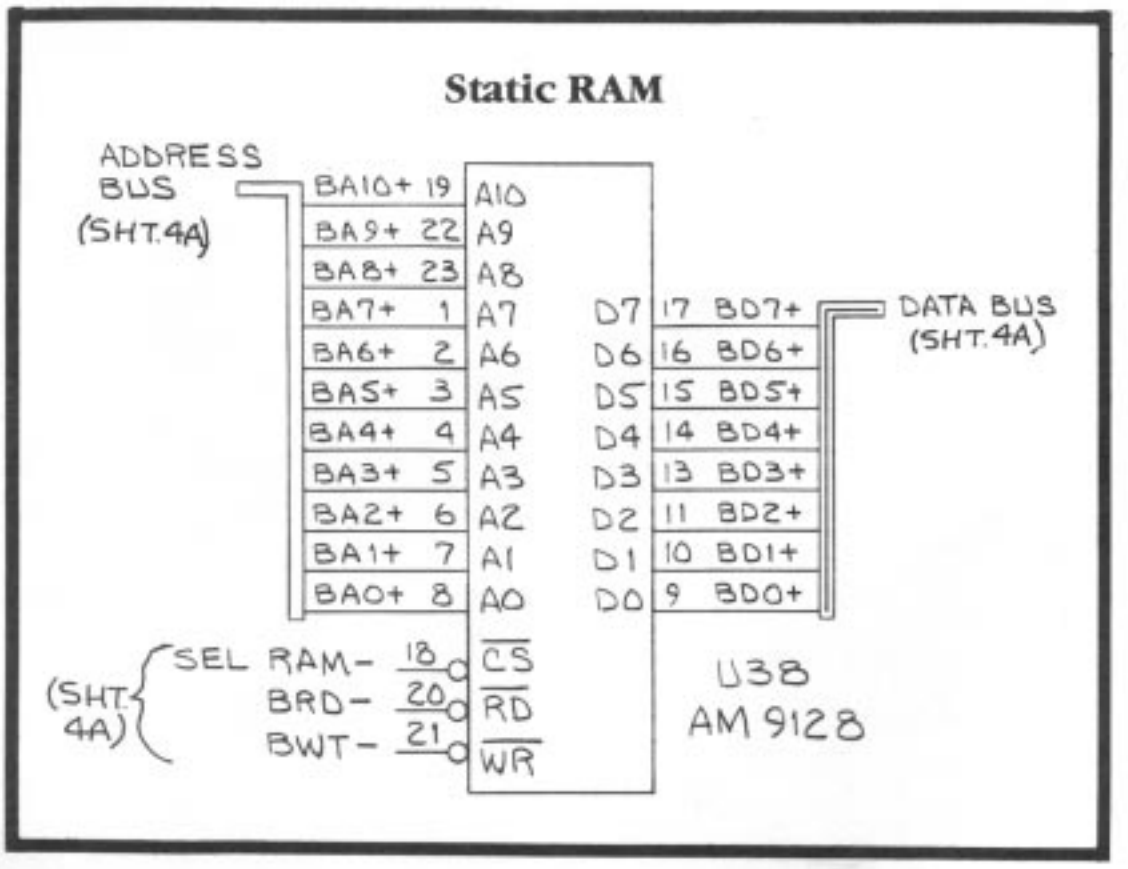
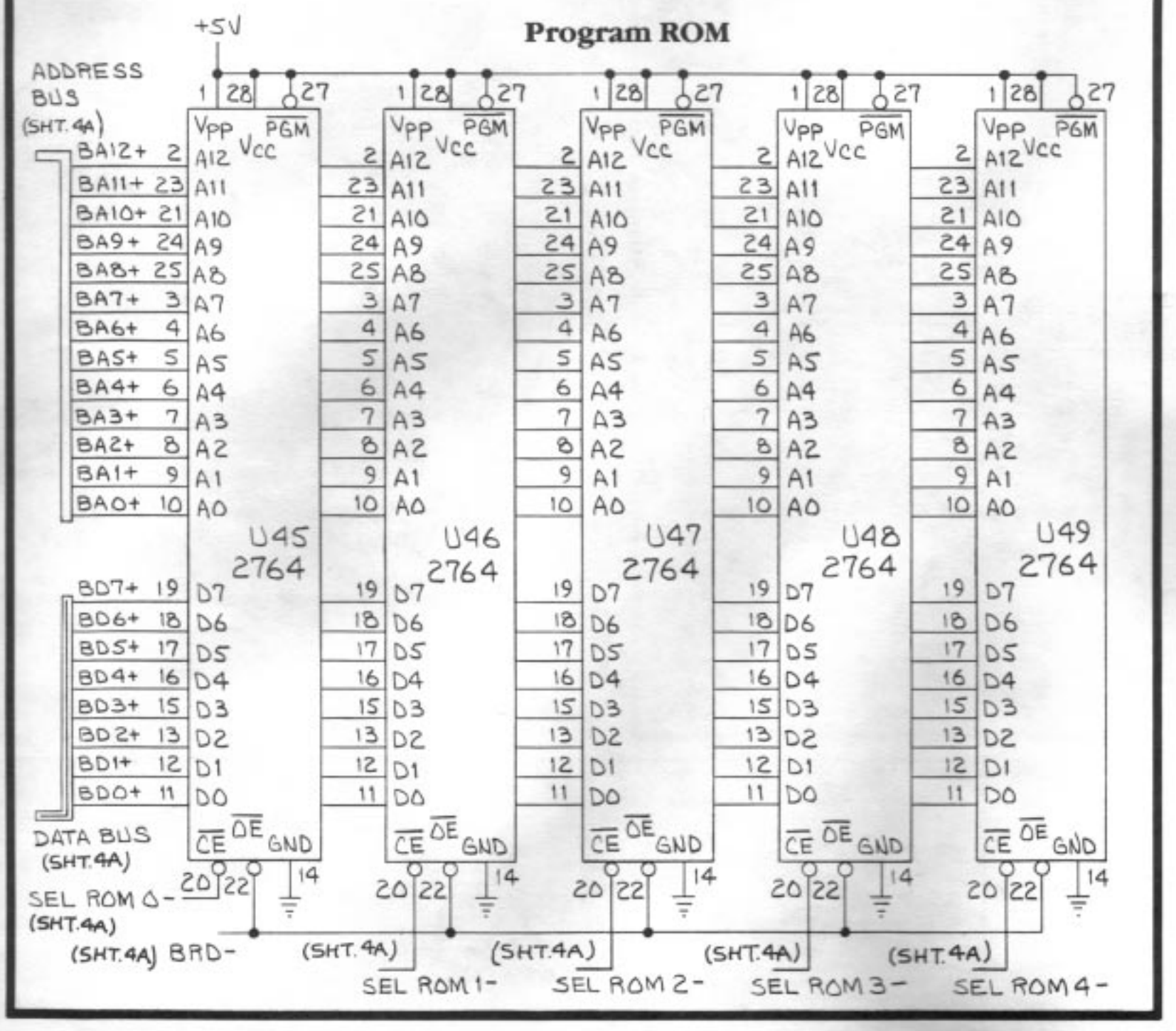
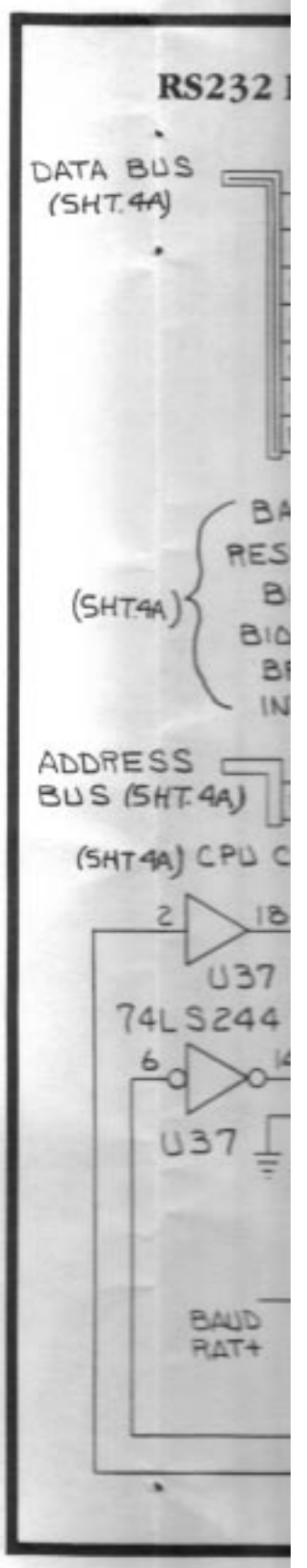
Static RAM

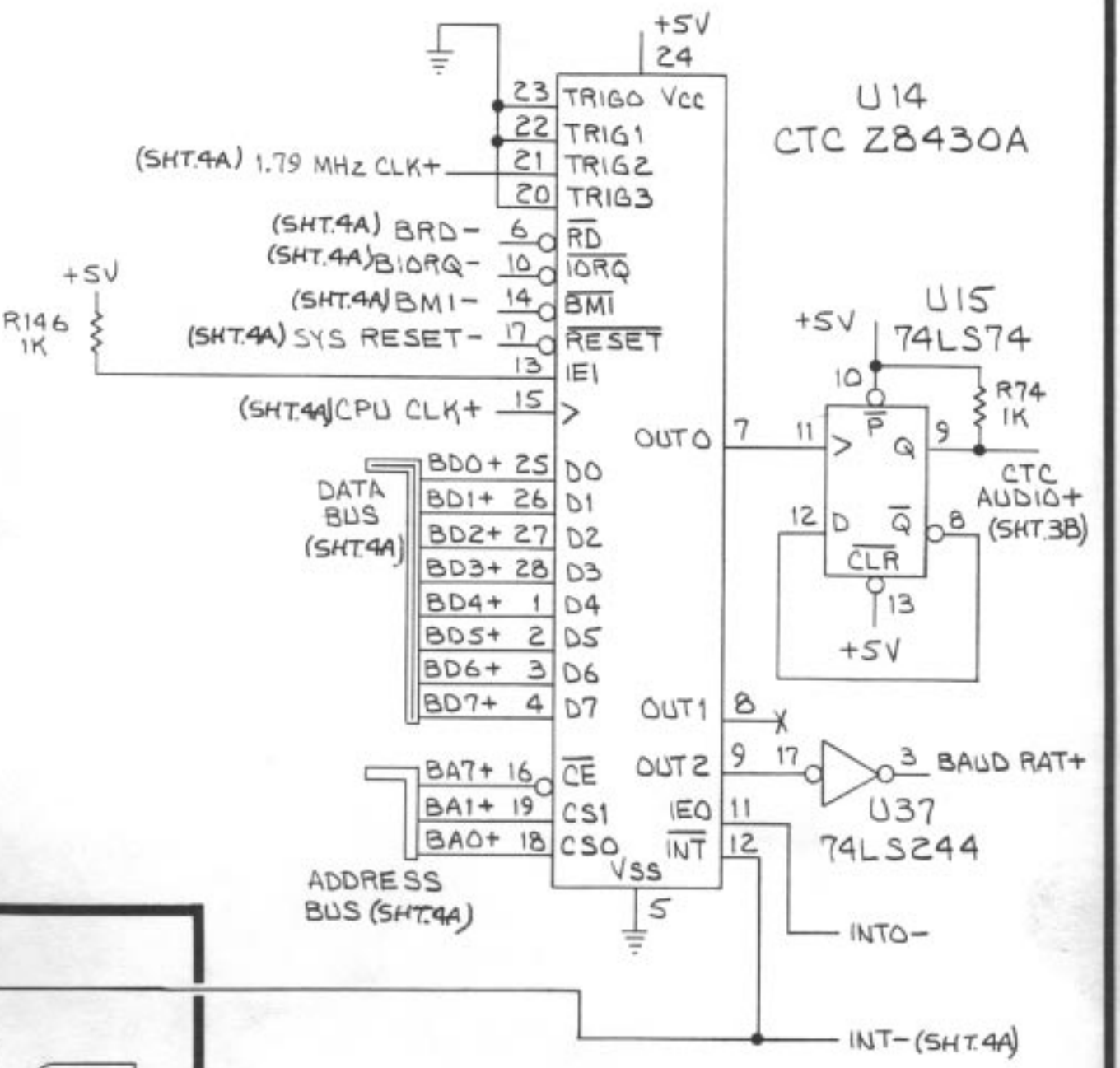


Program ROM

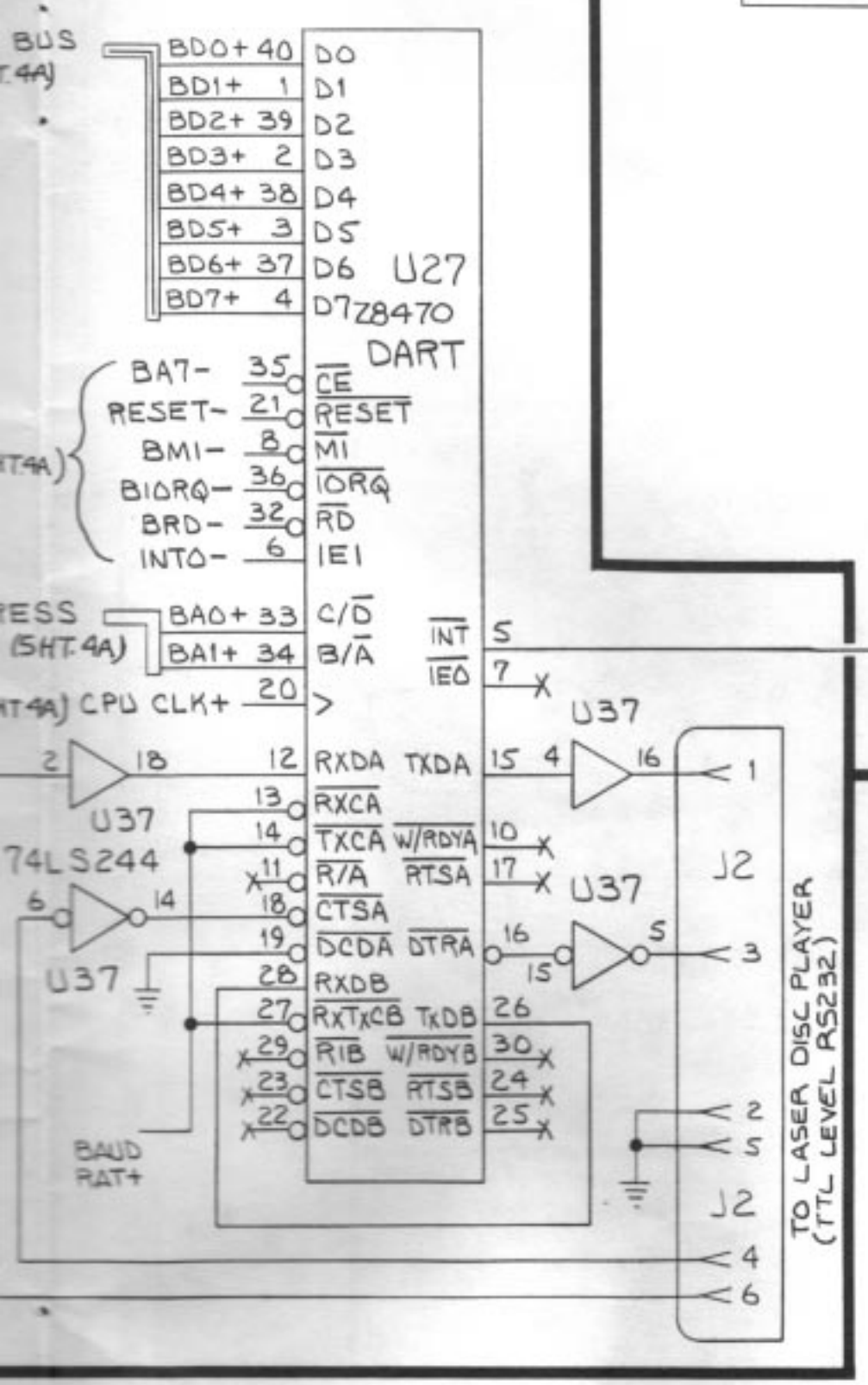




Counter/Timer/Audio



RS232 Interface



Dragon's Lair Main PCB
Schematic Diagram

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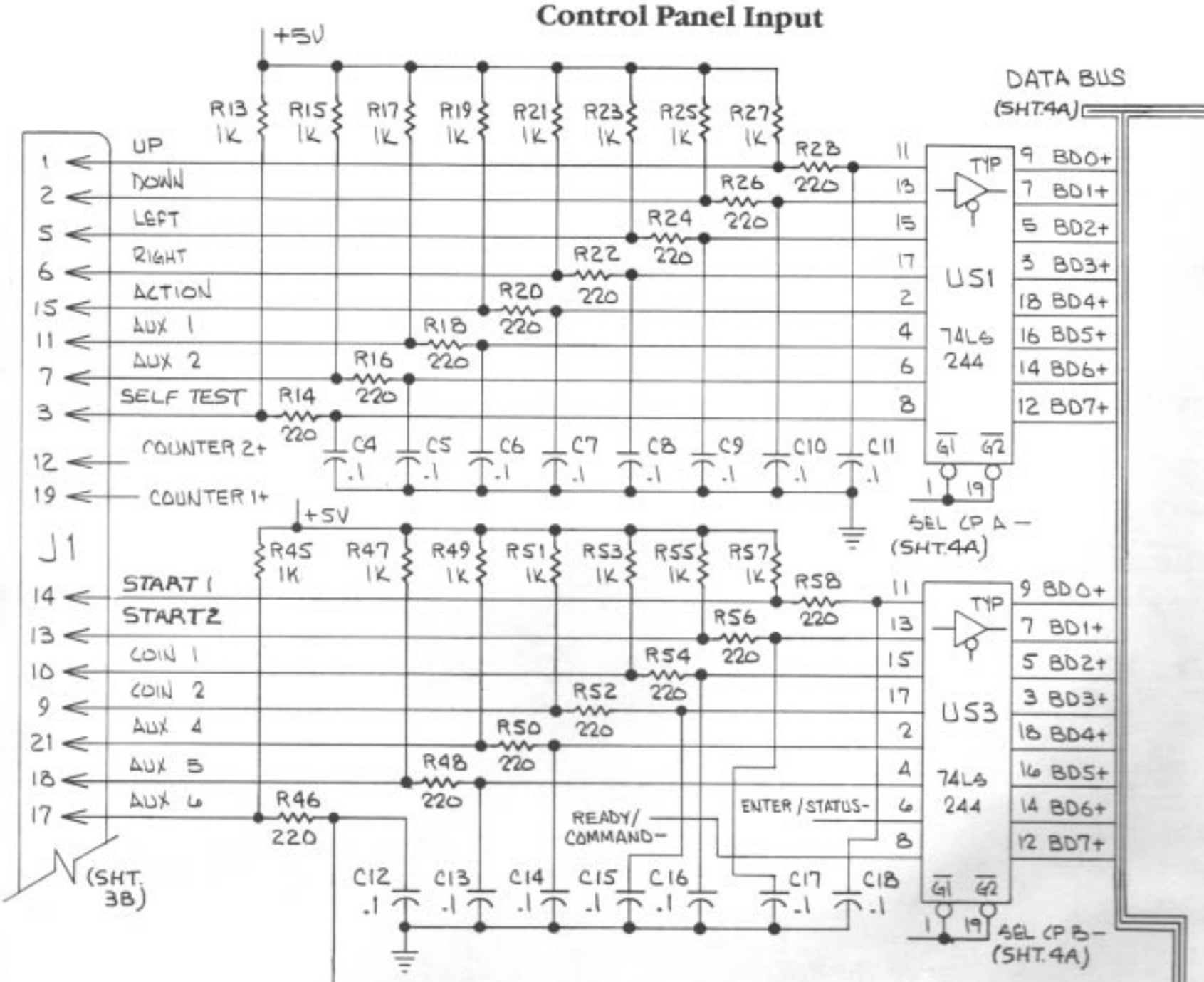
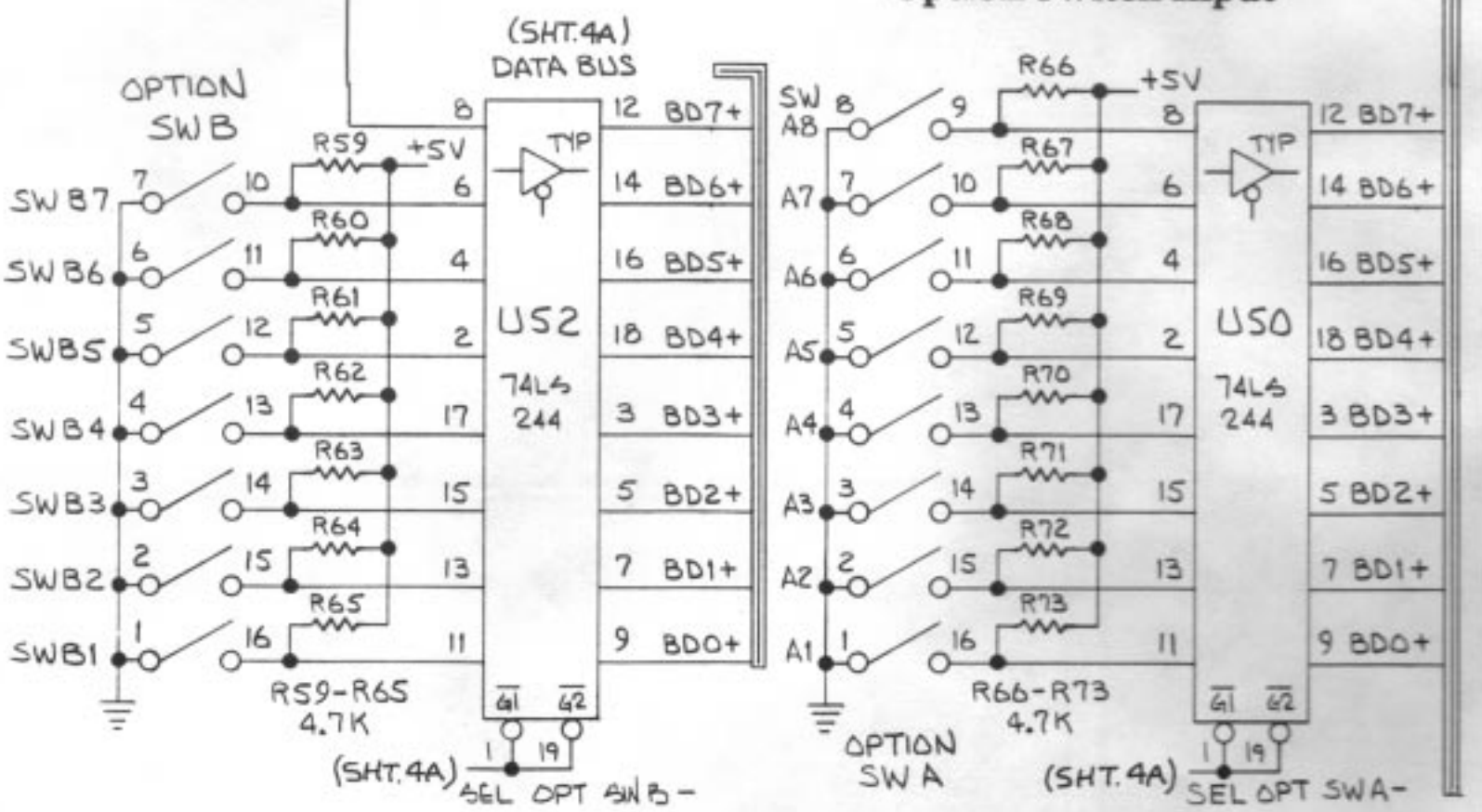
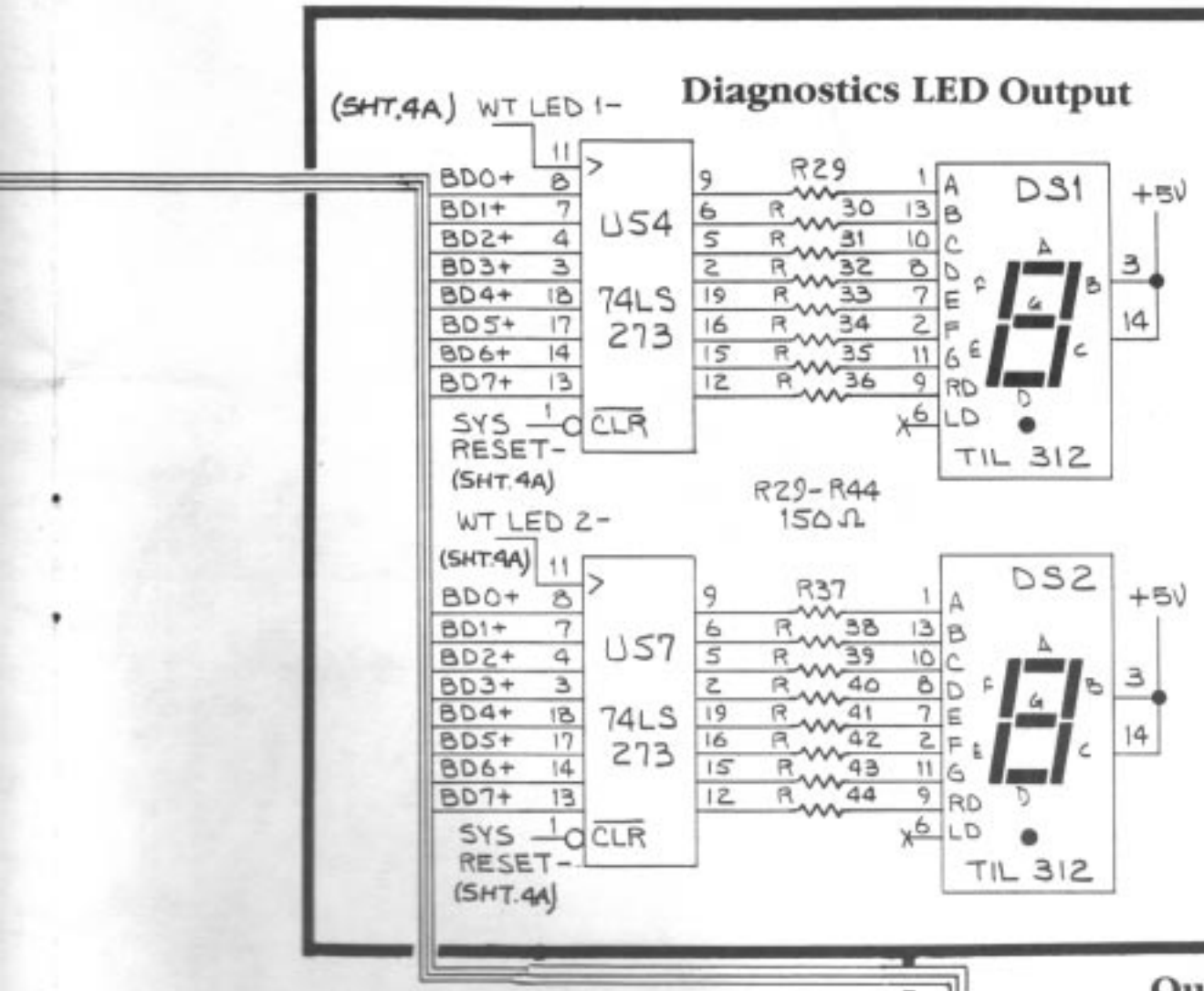
Control Panel Input



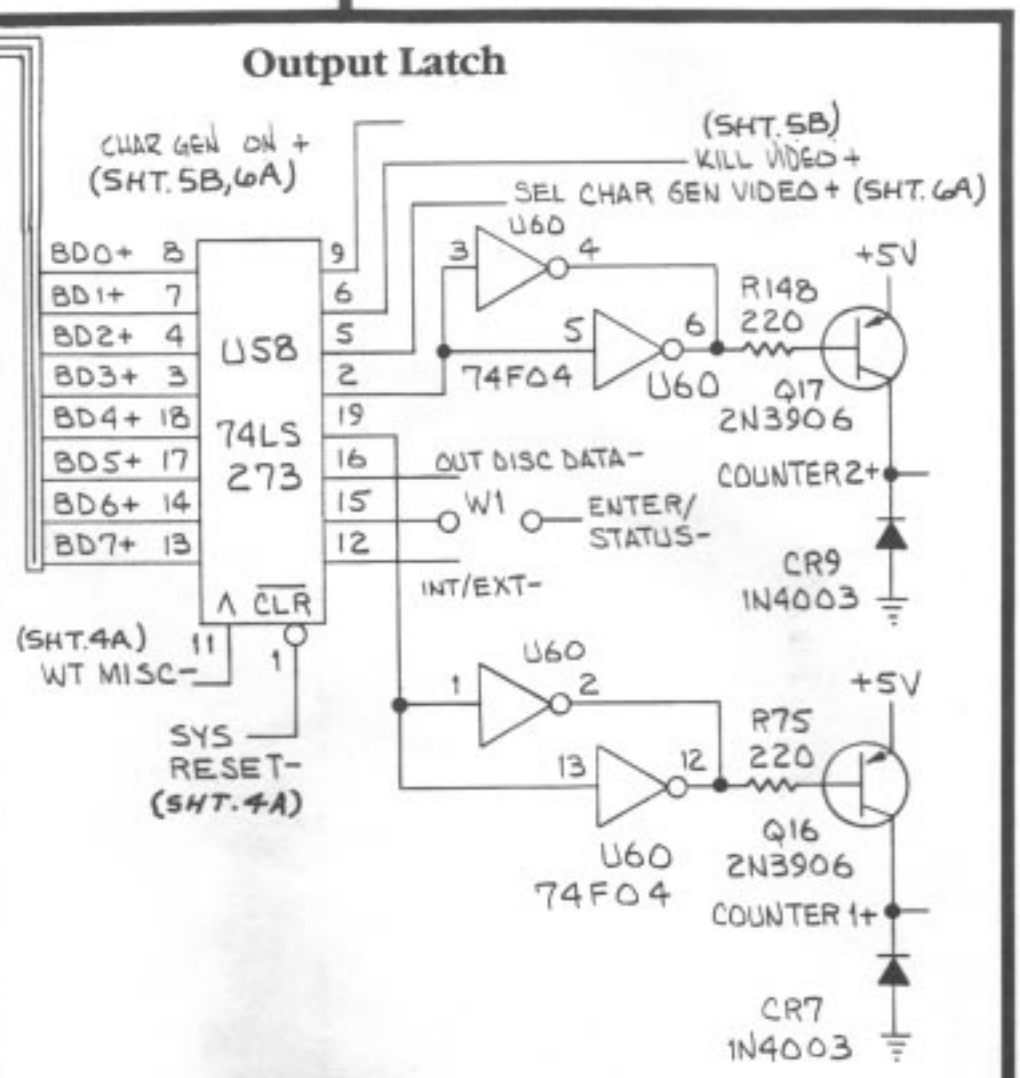
Option Switch Input



Diagnostics LED Output



Output Latch



Dragon's Lair Main PCB Schematic Diagram

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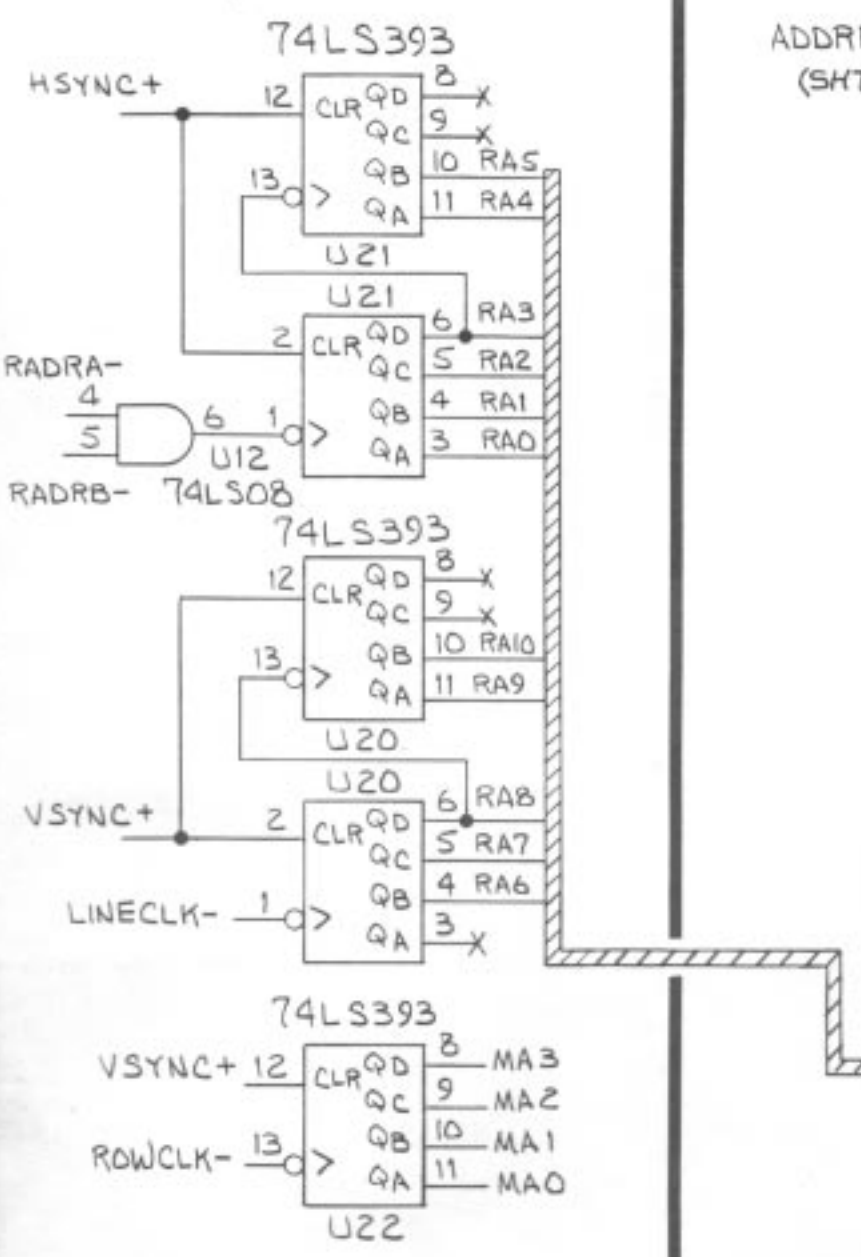
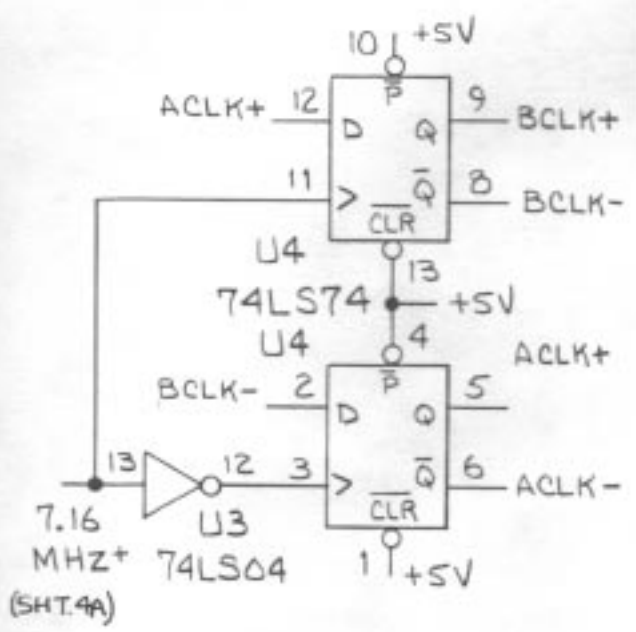
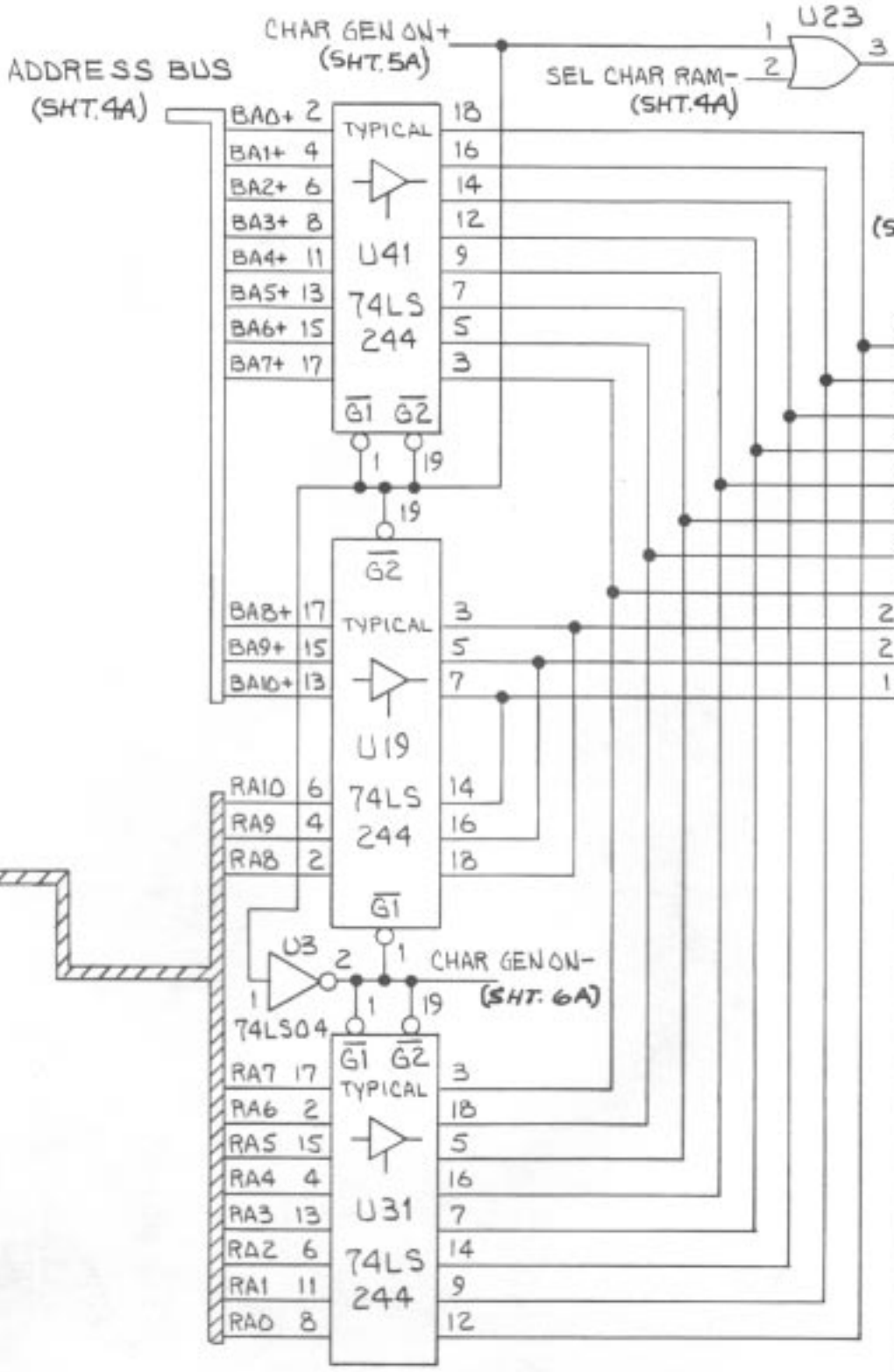
Sync Chain



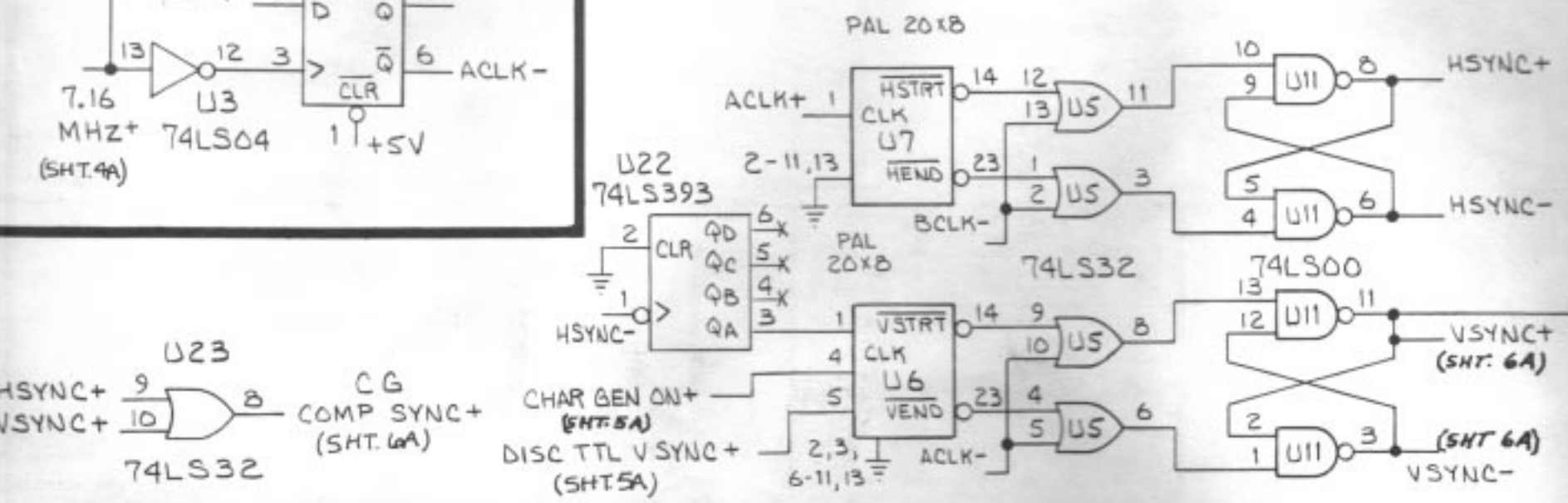
Video Clock

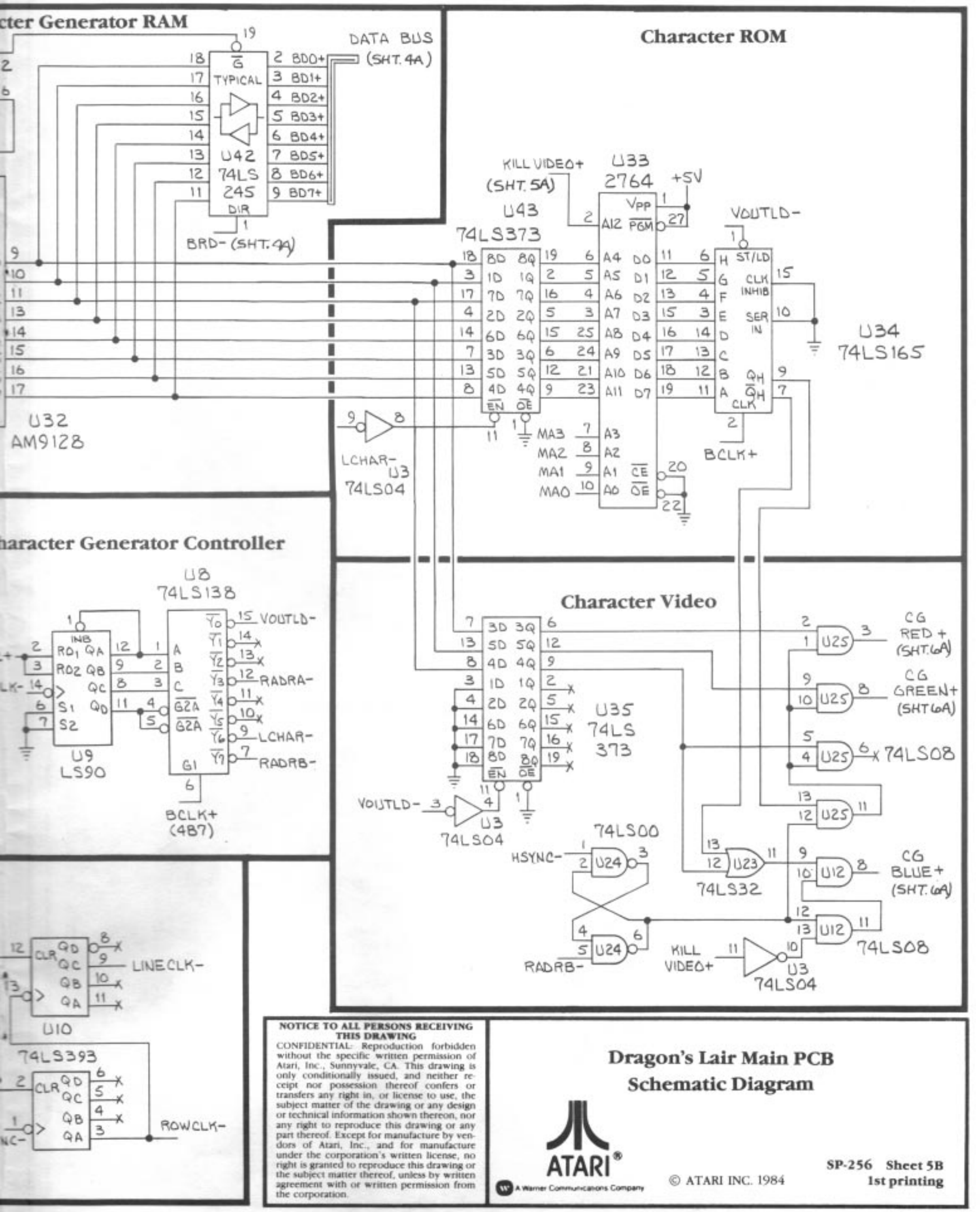


Character Ge



Vertical and Horizontal Sync





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Dragon's Lair Main PCB
Schematic Diagram

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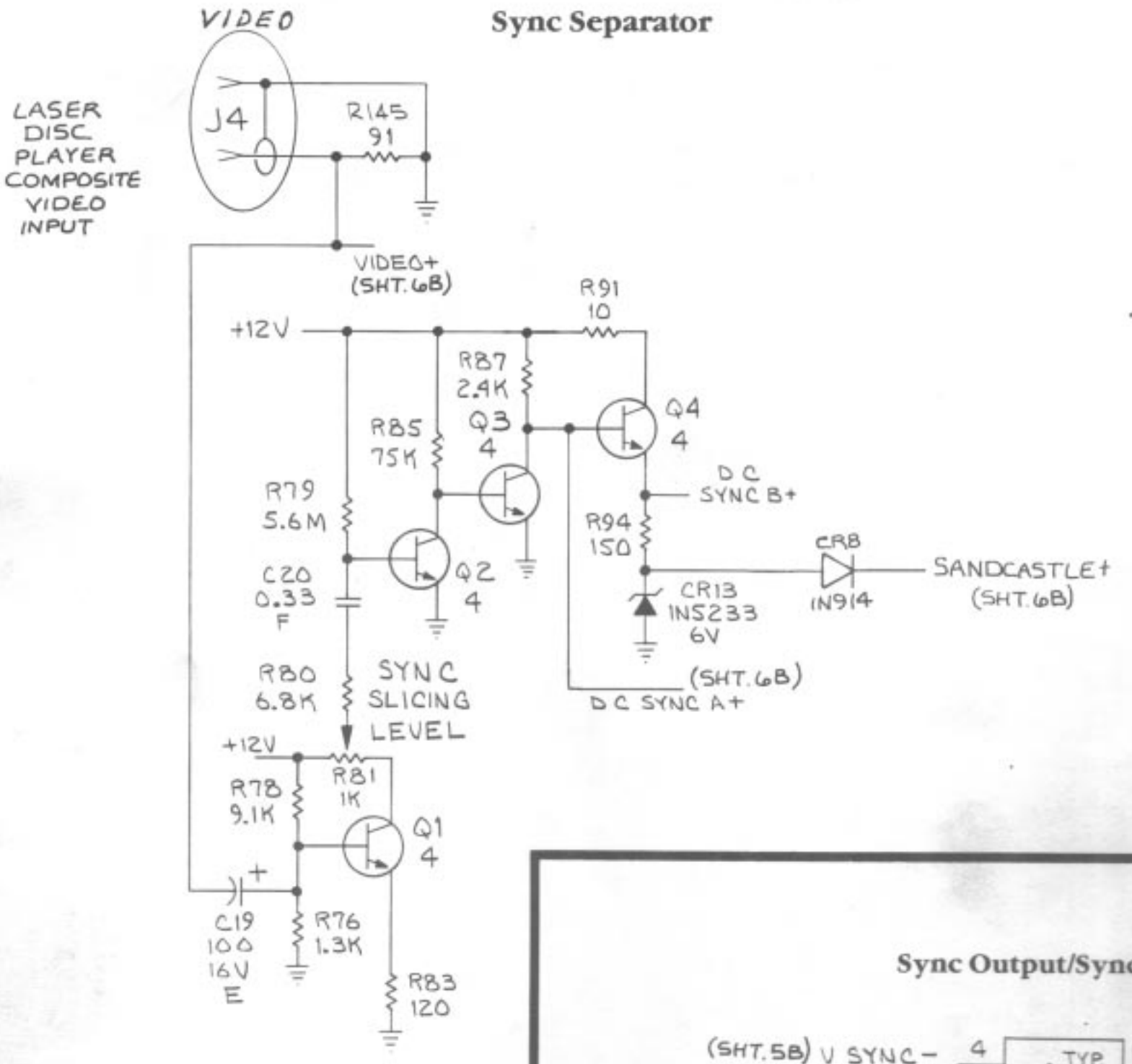
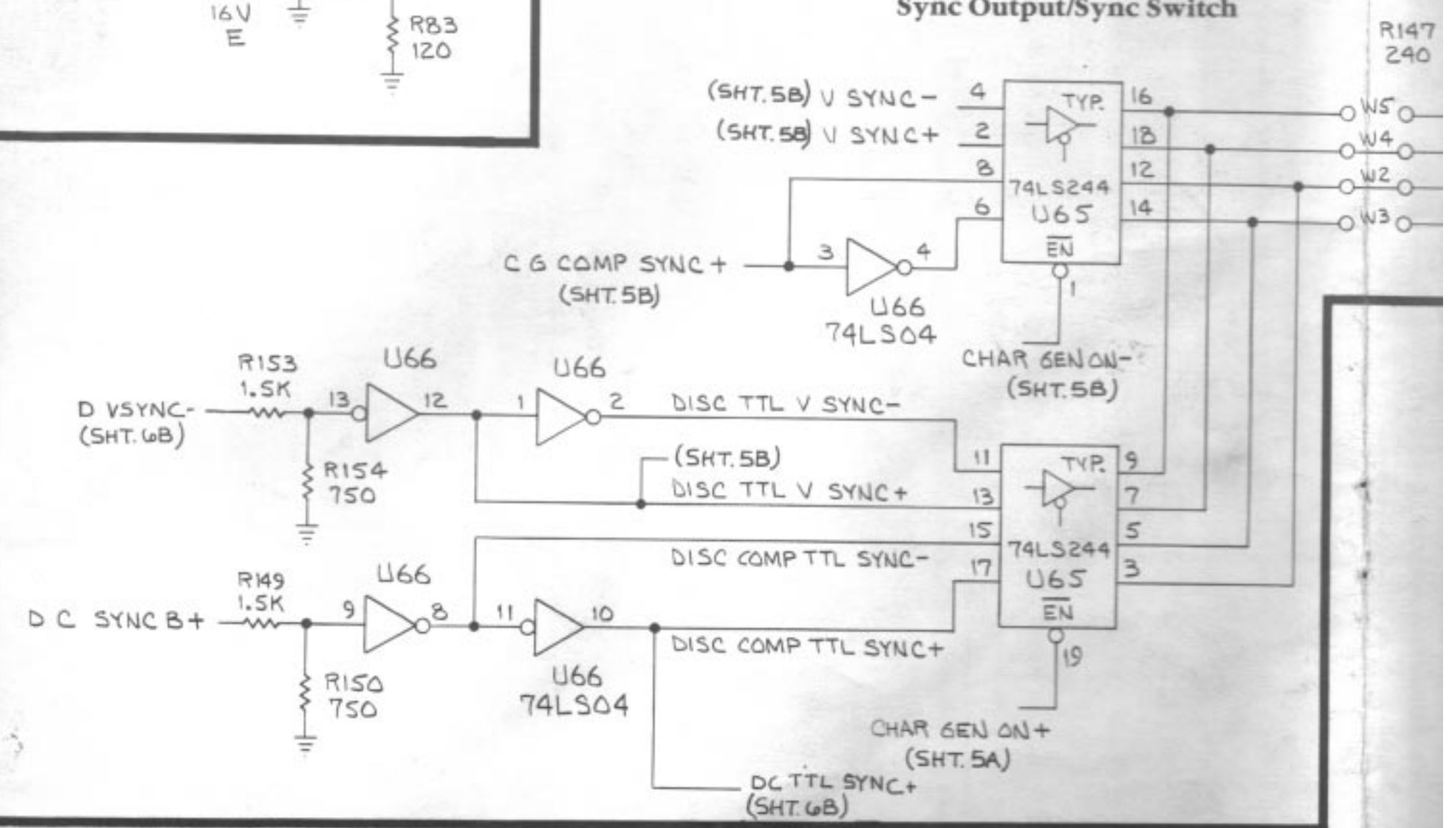
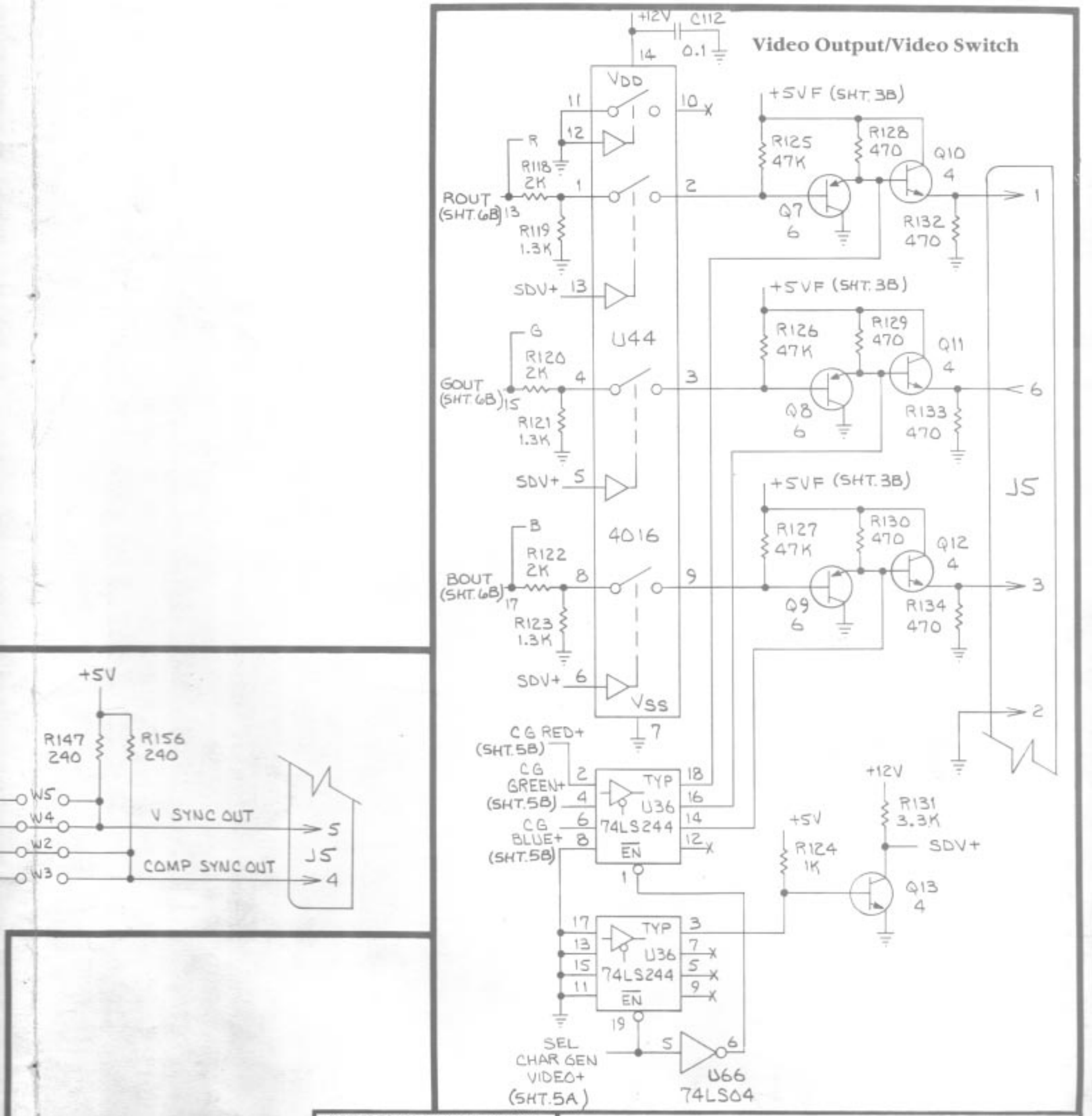
Sync Separator



Sync Output/Sync Switch





Dragon's Lair Main PCB
Schematic Diagram

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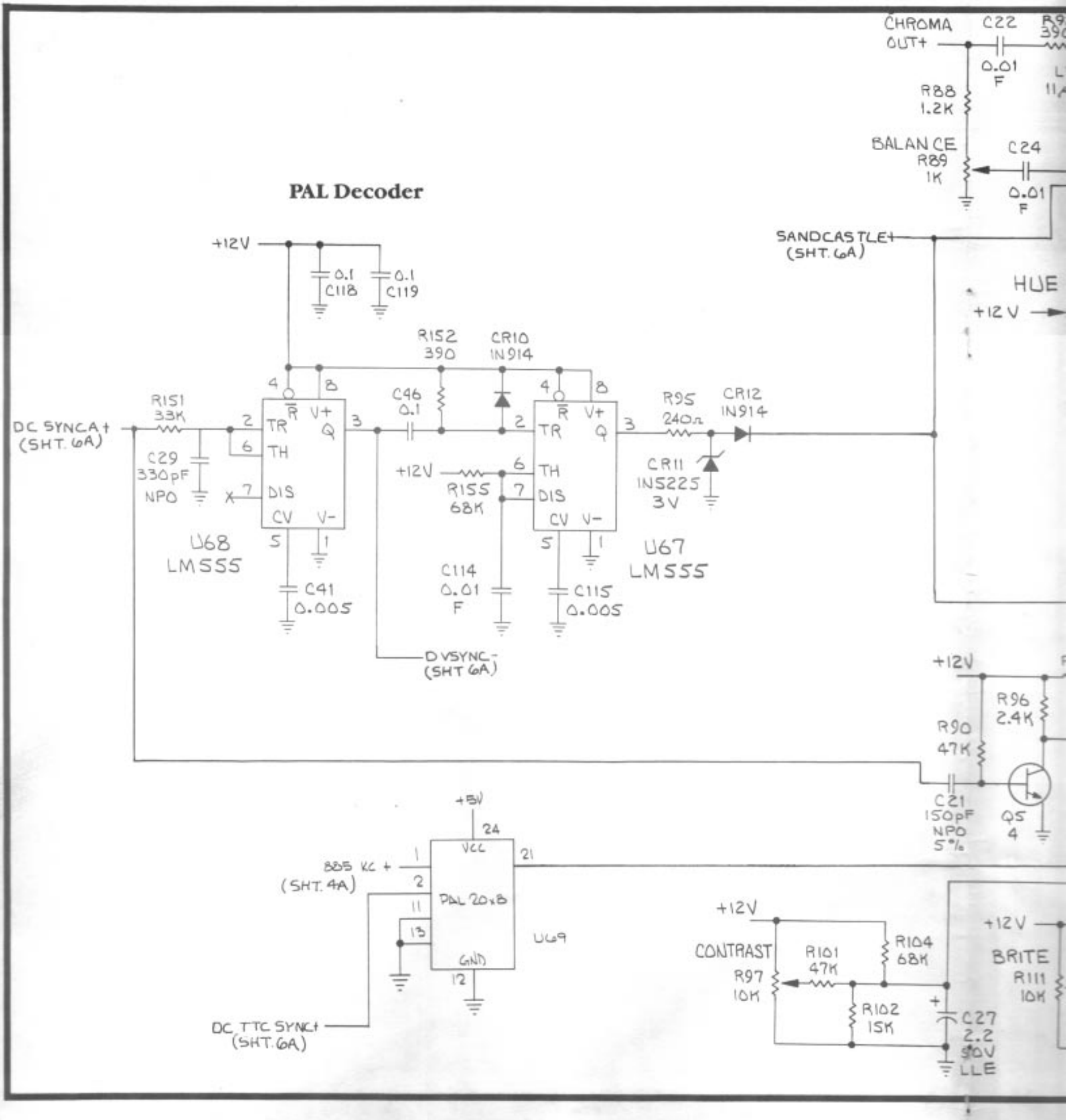
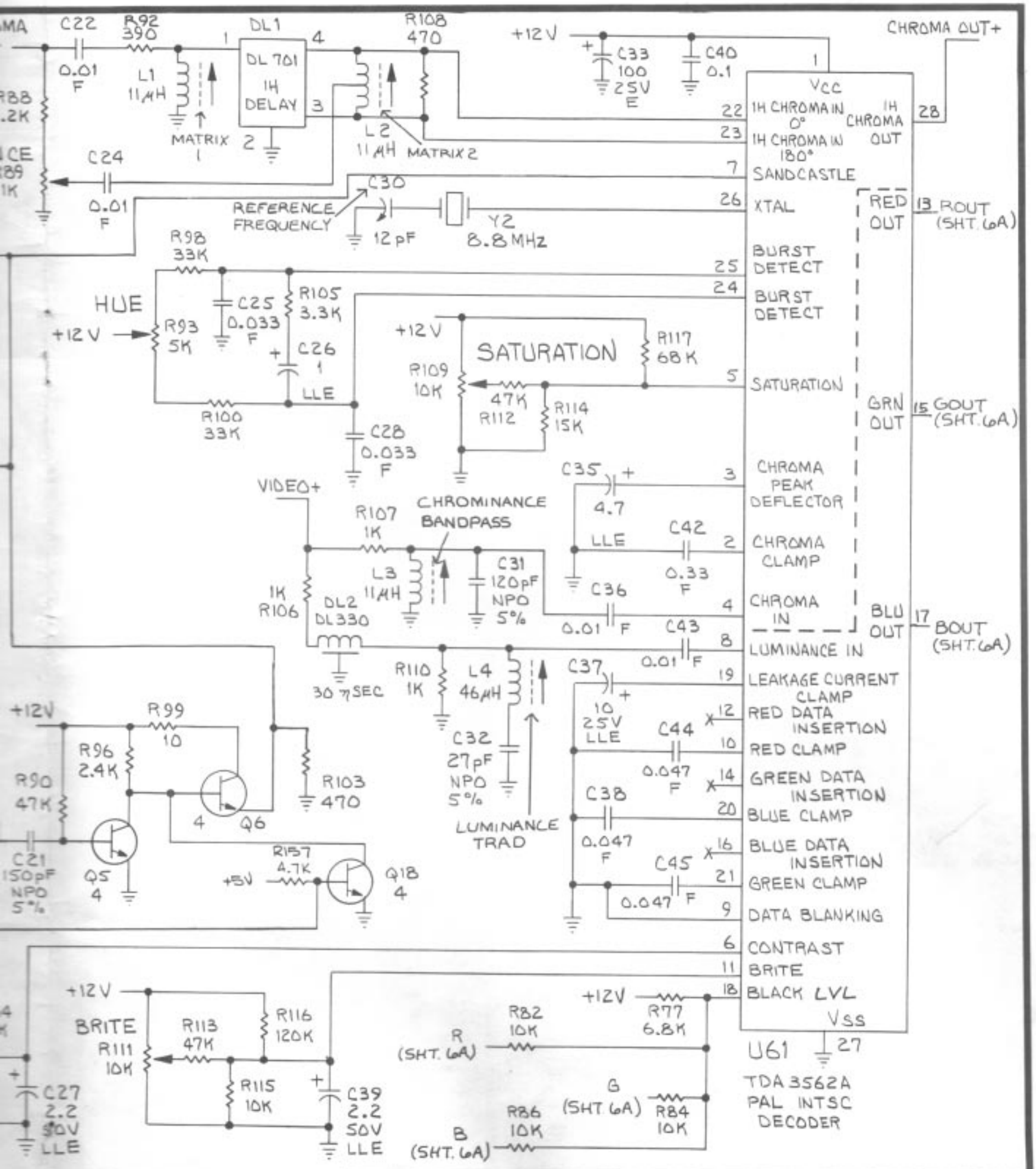
PAL Decoder


CHROMA OUT+
C22
0.01 F
R88 1.2K
BALANCE R89 1K
C24
0.01 F
SANDCASTLE+ (SHT. 6A)
HUE
+12V
+12V
0.1 C118
0.1 C119
R152 390
CR10 IN914
DC SYNCA+ (SHT. 6A)
R151 33K
C29 330pF NPO
C46 0.1
R95 240Ω
CR12 IN914
CR11 IN5225 3V
R155 68K
U68 LM555
U67 LM555
C41 0.005
C114 0.01 F
C115 0.005
DVSYNC- (SHT 6A)
+12V
R96 2.4K
R90 47K
C21 150pF NPO 5%
Q5 4
+5V
885 KC+ (SHT. 4A)
PAL 20x8
U69
DC TTC SYNC+ (SHT. 6A)
+12V
CONTRAST
R97 10K
R101 47K
R104 68K
R102 15K
C27 2.2 50V
+12V
BRITE
R111 10K



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Dragon's Lair Main PCB
Schematic Diagram

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SP-256 Sheet 6B
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THEORY OF OPERATION

The Main printed circuit board (PCB) is divided into three major sections: the controller, the character generator, and the video demodulator. The following discussion contains parenthetical name and sheet number references to the major circuits outlined on the schematic diagrams. Refer to these referenced schematic diagrams to aid in understanding the operation of the Main PCB circuitry.

Controller

This section of the Main PCB controls the game play by reading the switch inputs and controlling the disc player and character generator. The central processing unit (CPU) is comprised of Z80A microprocessor U29 (see Microprocessor, sheet 4A). The microprocessor clock (see Microprocessor Clock, sheet 4A) generates a 14.31818-MHz squarewave and consists of integrated circuit U18, 14.31818-MHz crystal Y1, resistors R5 and R6, and capacitors C2 and C3. The clock signal is fed to integrated circuit U2 where it is divided by two to provide a 7.16-MHz clock signal used in the character generator; divided by four to provide a 3.58-MHz clock signal through integrated circuit U37 to pin 6 of microprocessor U29; divided by 16 and fed through integrated circuits U2, U1, and U16 (see Watchdog and Reset, sheet 4A) to provide a wathchdog timer which is used to reset microprocessor U29. The reset circuit, comprised of transistor Q15, reset pushbutton switch S1, and associated circuitry, also provides manual reset for microprocessor U29. A reset pulse at pin 26 of microprocessor U29 clears its registers and begins program execution at the first location in memory. Thus, reset can occur during power up, when reset switch S1 is actuated, or when program execution is abnormally halted. Dip switch SW B-8 enables/disables the watchdog timer.

The data, address, and control busses are recognized by microprocessor U29. The data bus is bidirectional and is buffered by U28 (see Microprocessor, sheet 4A). Bus direction is determined by control bus signals to gate U17, after buffering by U40. The address bus is unidirectional only and is buffered by U30 and U39. Integrated circuits U59, U63, and U64 perform address decoding for the entire system (see Address Decoder, sheet 4A).

The program ROM is comprised of integrated circuits U45 through U49 (see Program ROM, sheet 4B) which are 64K-bit erasable programmable read-only memories (EPROM). Each of these integrated circuits provides 8K bytes of memory for a total of 40K bytes of memory. Integrated circuit U38 is a static RAM that provides general random access memory for the Z80A (see Static RAM, sheet 4B).

Counter timer circuit (CTC) U14 provides vectored interrupts for real-time processes, clock signals for serial communication, and audio (see

Counter/Timer/Audio, sheet 4B). Audio output from pin 7 of U14 is fed to flip-flop U15, which provides a symmetrical audio square wave to dual asynchronous receiver of transmitter (DART) U27 (see RS232 Interface, sheet 4B). The clock output from pin 9 of U14 supplies a baud-rate clock signal generated from the 1.79-MHz clock signal applied to pin 21 from U2 in the clock circuit of microprocessor U29. The baud-rate clock signal at pin 9 of U14 is fed through buffer U37 to pins 13, 14, and 27 of U27.

Dual asynchronous receiver or transmitter U27 is used for communications with serially-interfaced disc players. The outputs at pin 1 and 3 of connector J2 are serial TTL data and status to the disc player. The inputs at pins 4 and 6 of J2 are status and receive data from the disc player. Actual protocol is in software in RS232 format and at TTL signal levels.

Integrated circuits U51 and U53 are used to read control panel inputs (see Control Panel Input, sheet 5A). The resistor-capacitor networks at the inputs to the buffers are required for input conditioning and electrostatic discharge protection. Pins 6 and 8 of U53 are used for handshaking inputs from parallel-interfaced disc players.

Integrated circuits U52 and U50 are used to read option switches SW A and SW B (see Option Switch Input, sheet 5A). Integrated circuits U54 and U57 with LEDs DS1 and DS2 provide the printed circuit board LED display function (see LED Output, sheet 5A). Integrated circuit U58 (see Output Latch, sheet 5A) is used to provide miscellaneous latched external interface (e.g., coin-counter output, parallel disc player handshaking, and interface to the character generator for control).

Character Generator

The character generator provides display messages at certain intervals (e.g., score, coinage, and additional information).

Microprocessor U29 controls the character generator with the CHAR GEN ON signal at pin 9 of register U58 (see Output Latch, sheet 5A). The CHAR GEN ON signal is used to multiplex data and address lines to the character generator 2K static RAM U32 (see Character Generator RAM, sheet 5B). When pin 9 of U58 is active high, buffer U31 and the bottom half of buffer U19 are accessing the RAM address lines, and the RAM data outputs are fed to registers U35 and U43 (see Character Video and Character ROM, sheet 5B).

If the CHAR GEN ON signal is active low, buffer U41, the top half of buffer U19, and buffer U42 can access the RAM U32 data and address lines (see Character Generator RAM, sheet 5B) to allow microprocessor U29 to write instructions for the character generator into the RAM U32 memory.

The 7.16-MHz signal from pin 11 of counter U2 provides the clock for the character generator through flip-flop U4 (see Video Clock, sheet 5B). The ACLK (A clock) and BCLK (B clock) outputs from U4 are 3.58-MHz clock signals that are phased 90° apart.

The A clock generally provides logic transition, while the B clock allows output states to settle. The A and B clock signals produce other clock signals that are actually used to drive the system through counter U9 and multiplexer U8, which provide an 8-step clock signal (see Character Generator Controller, sheet 5B), and through PAL integrated circuits U6 and U7 (see Vertical and Horizontal Sync, sheet 5B), which provide horizontal and vertical sync pulses. The outputs of U6 and U7 are fed through gate U5 to remove noise and through flip-flop U11 to provide the appropriate signal length. The vertical sync pulses feed the display and clear most of the address counters. Tri-state buffer U65 has additional inputs of disc TTL-level vertical sync and CHAR GEN ON signals which switch the sync pulses between the two video sources (see Sync Out/Sync Switch, sheet 6A).

The sequence clock signal from U8 and U9 is used to enable registers and latches. Counters U20, U21, and U22 generate display address information for the character generator RAM (see Sync Chain, sheet 5B). Register U43 latches data output from RAM U32 and presents it as address inputs to ROM U33 (see Character ROM, sheet 5B). ROM U33 contains detailed pixel information for each of the characters to be displayed. Data output from U33 is fed to parallel-in/serial-out shift register U34, which clocks out data for display. Register U35 determines the color of the character (see Character Video, sheet 5B). Flip-flop U24 suppresses the output of the first character on each line. Gate U25 and half of gate U12 multiplex data and color information to provide output video from the character generator.

Video Demodulator

The video demodulator is comprised of PAL decoder U61, which functions as a chrominance/luminance processor for the PAL composite video (see PAL Decoder, sheet 6B). Video input is routed through connector J4 to the sync separator circuit comprised of transistors Q1 through Q6 and Q18, which provide the disc sync and sandcastle pulse used by PAL decoder U61 to gate color burst.

Input video is also routed through the band-pass filter comprised of resistor R107, inductor L3, and capacitor C31 to extract chrominance information; then, through resistor R106, delay line DL2, resistor R110, and inductor L4 to extract luminance information.

The remainder of the circuit consists of external capacitance for the processor crystal input, saturation, hue, brightness and contrast controls, and video delay line DL1, which is used in the PAL demodulation circuit to correct tint. The output from processor U61 provides direct drive for the red, green, and blue guns. Integrated circuit U44 is a switching device used

to switch from decoder output to character generator output (see Video Output/Video Switch, sheet 6A). Transistors Q7 through Q12 are used to condition the signal output and drive the display through connector J5.

Miscellaneous

Additional circuits on the Main PCB consist of a voltage-regulator and audio-amplifier (see Power Input and Audio Amp/Output, sheet 3B). The regulator comprised of rectifiers CR3, CR5, and CR6, capacitors C51, C52,

C57, C60, C64, and C69, regulator VR2, and inductor L5 provides +12 and +5 volts to the video decoder section of processor U61. The regulator comprised of regulator VR1, capacitors C50 and C112, resistor R135, transistor Q14, and rectifier CR4 provides input voltages for audio amplifiers U13 and U26. Digitally-generated audio from sound processor U14 (see Counter/Timer/Audio, sheet 4B) is fed through connector J1 to volume control B and back to audio amplifier U26.

Dragon's Lair Theory of Operation, cont.

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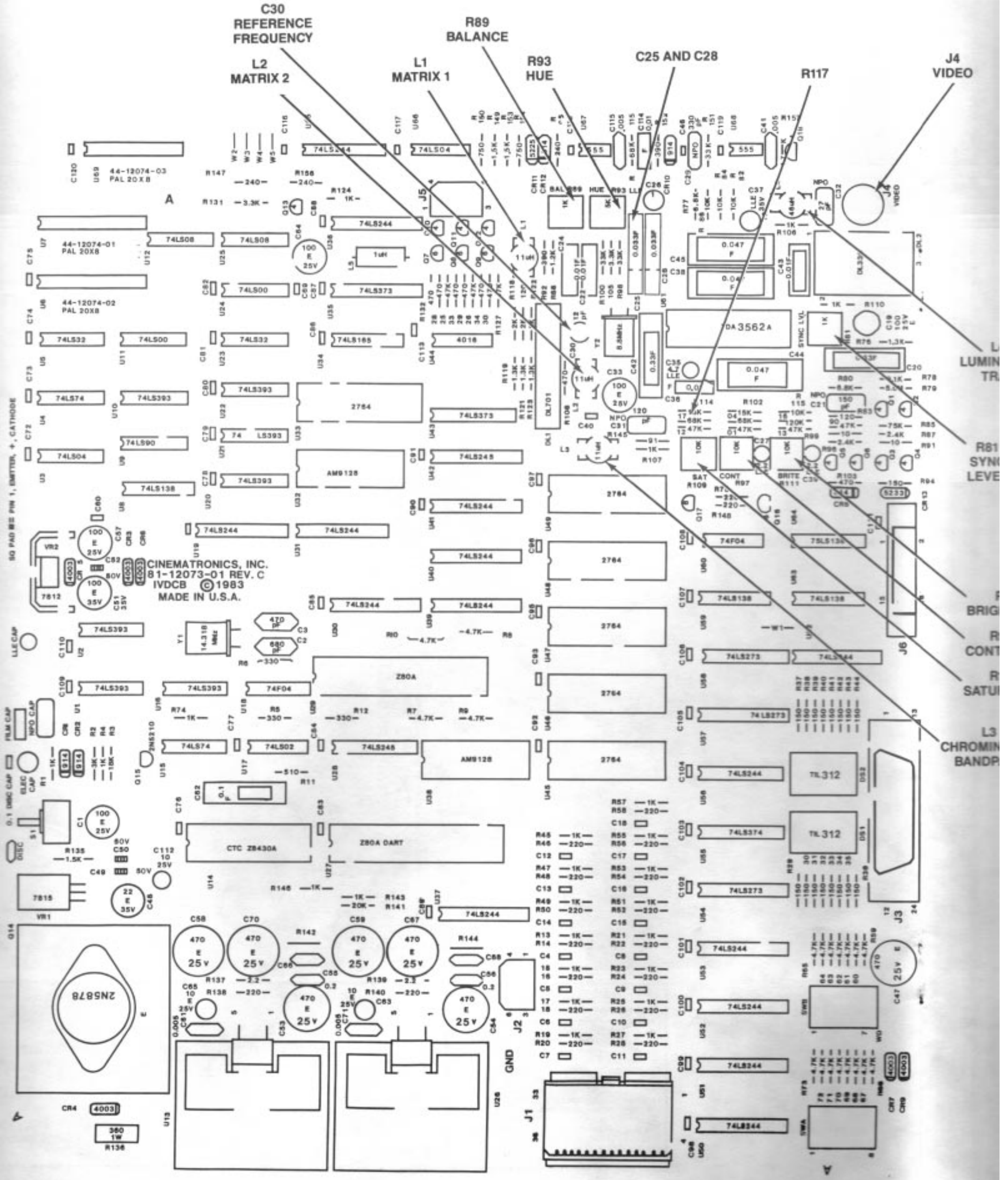
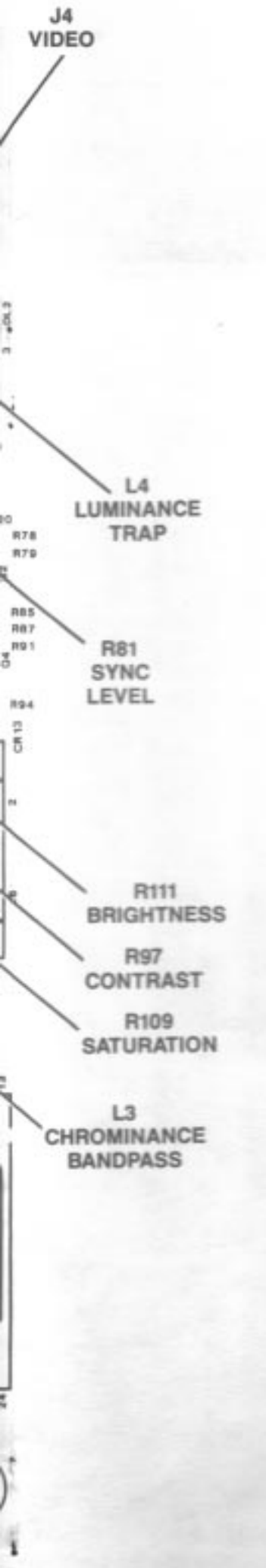

C30
REFERENCE
FREQUENCY
L2
MATRIX 2
L1
MATRIX 1
R89
BALANCE
R93
HUE
C25 AND C28
R117
J4
VIDEO
CINEMATRONICS, INC.
81-12073-01 REV. C
IVDCB ©1983
MADE IN U.S.A.
44-12074-03
PAL 20X8
44-12074-01
PAL 20X8
44-12074-02
PAL 20X8
74LS244
74LS504
74LS08
74LS00
74LS373
74LS32
74LS165
4016
74LS393
74LS74
74LS90
74LS138
74LS245
AM9128
2764
74LS04
74F04
Z80A
Z80A DART
CTC Z8430A
74LS502
74LS374
74LS273
TIL312
DA3562A
2N5878
7812
7815
14.318 MHz
6.5MHz
SAT
CONT
BRITE
J1
J2
J3
J4
J5
J6
GND



ADJUSTMENT PROCEDURE

The sync separator and PAL decoder circuits are adjusted before shipment from Atari. These circuits should require adjustment only after repair or replacement. Refer to the Adjustment Locations illustration on this sheet to aid in locating the adjustments and other components mentioned in the following procedures.

Test Equipment Required

1. PAL color-bar generator
2. Non-metallic inductor tuning tool
3. Oscilloscope
4. Jumpers (E-Z Hooks)

Preliminary Procedure

1. Turn off the game power.
2. Disconnect the composite video from the laser disc player at BNC connector J4 (VIDEO) on the Main PCB.
3. Connect the video output from the PAL color bar generator to BNC connector J4 (VIDEO) on the Main PCB.
4. Connect a jumper across resistor R117 to apply +12V directly to pin 5 of PAL decoder U61.
5. Short across pins 24 and 25 of PAL decoder U61 by connecting a jumper between the noncommon ends of capacitors C25 and C28.
6. Turn on the game power.

Reference Frequency

1. Perform the Preliminary Procedure.
2. Adjust C30 (REFERENCE FREQUENCY) for a minimum number of horizontal bands and roll in the game display.
3. Switch the game power off and on again.
4. Repeat steps 2 and 3 until the number of horizontal bands and roll is reduced to a minimum.

Dragon's Lair Adjustment Procedures

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Chrominance Bandpass

1. Perform the Preliminary Procedure.
2. Connect an oscilloscope probe to pin 28 of PAL decoder U61.
3. Adjust L3 (CHROMINANCE BANDPASS) for maximum signal amplitude on the oscilloscope display.

Luminance Trap

1. Perform the Preliminary Procedure.
2. Connect an oscilloscope probe to pin 15 of PAL decoder U61 (GRN OUT).
3. Adjust L4 (LUMINANCE TRAP) for minimum 4.4-MHz carrier on the displayed oscilloscope waveform.

PAL Matrix

1. Perform the Preliminary Procedure.
2. Connect an oscilloscope probe to pin 15 of PAL decoder U61 (GRN OUT).
3. Apply two consecutive anti-PAL signal lines from the PAL color bar generator.
4. Adjust L1 (MATRIX 1), L2 (MATRIX 2), R89 (BALANCE), and R93 (HUE) for the best match between the two consecutive video lines displayed on the oscilloscope (i.e., minimum color in the gray scale on the game display).

Contrast, Brightness, and Saturation

1. Perform steps 1 through 3 of the Preliminary Procedure.
2. Turn on the game power.
3. Adjust R97 (CONTRAST) and R111 (BRIGHTNESS) for acceptable contrast and brightness on the game display.
4. Adjust R109 (SATURATION) for best color saturation on the game display.

Sync Slicing Level

1. Perform steps 1 through 3 of the Preliminary Procedure.
2. Turn on the game power.
3. Adjust R81 (SYNC LEVEL) fully clockwise for optimum sync locking on the game display.

Dragon's Lair Adjustment Procedures, cont.

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