

# FREEDOM FIGHTER

**MILLENNIUM**  
GAMES PRODUCTS  
A Subsidiary of Malibu Grand Prix Corp.

FREEDOM FIGHTER™  
OPERATION and SERVICE MANUAL  
1st Edition

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## FCC NOTICE & WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply within the limits for a Class A computing device pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

## WARRANTY

The FREEDOM FIGHTER<sup>TM</sup> game parts are warrantied for a period of 90 days from the date of purchase, except for the disk player motor which is warrantied for a period of one (1) year from the date of purchase. The warranty includes the cost of labor but not the cost of shipping of any parts and/or repaired items. When calling for warranty repairs or parts you MUST have your serial number and date of purchase. Do not send any repair boards or return parts without first obtaining an RMA number from the customer service department.

## QUESTIONS

MILLENNIUM GAMES PRODUCTS asks technicians to use the customer service phone line for any questions they may have regarding the FREEDOM FIGHTER<sup>TM</sup> game. That number is (818) 340-6750.

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## I. PRELIMINARY PROCEDURES

## 1. GAME INSPECTION

All MILLENNIUM GAMES PRODUCTS equipment is packaged in well-padded cardboard containers to prevent damage during shipment. Before signing the delivery receipt, you should follow this procedure.

a. Check for obvious damage and make certain that the physical piece count of the shipment matches the piece count on the Bill of Lading. These two procedures should always be done before signing the delivery receipt.

b. Shortages and/or obvious damage to the packaging on any given shipment should be noted in writing on the delivery receipt before signing for the delivery.

c. If concealed damage is suspected on any shipment, those packages believed to contain the damaged goods should be opened in the presence of the delivery person. If the goods have sustained concealed damage, a description of said damage should be noted in writing on the delivery receipt before signing for the delivery.

d. Never apply power to any game with noticeable damage.

## 2. VISUAL INSPECTION

a. Open the rear and front access doors with the appropriate keys provided.

b. Examine each major and electrical component thoroughly for scrapes, dents, broken or missing parts and loosened screws.

c. Check for loose cable connections.

d. Visually verify that all the integrated circuit devices (IC's) are plugged into the sockets and properly seated with no broken or bent IC pins.

e. If you find any damage during this inspection, file a claim with the carrier. Send a complete report of the damage to MILLENNIUM GAMES PRODUCTS.

## 3. FILING A CLAIM

To file a claim, follow this procedure.

a. Any and all damaged freight, including the packaging, should be retained by the consignee until a physical inspection of said freight can be made by a representative of the carrier involved.

## FREEDOM FIGHTER MANUAL

b. The claims manager for the carrier involved should be notified as soon as possible after the goods are received. Preferably, the carrier's claims manager should be notified within forty-eight (48) hours of receipt of the goods by the consignee. If warrantied, a written claim must be filed with the carrier involved. A detailed description of the damages must be provided including copies of the delivery receipt, bill of lading, inspection report, and invoice. The carrier to which a claim has been filed against is required by law to respond to said claim within thirty (30) days after receiving your claim and must reach a final disposition in the matter within one hundred twenty (120) days.

### 4. INSTALLATION

Planning the location of the game should involve both physical and electrical considerations. Such physical considerations concern the placement of the equipment with respect to these clearances:

HEIGHT 72.00 inches, 183 cm  
WIDTH 25.75 inches, 66 cm  
DEPTH 30.00 inches, 76 cm

NOTE: The game must have a 12" clearance to the rear of the game to insure proper ventilation.

An indoor, relatively dust-free environment is necessary, with proper conditions required of any electrical component. Electrical requirements are the availability of an AC outlet with the correct voltage and frequency, 120 VAC-60 HZ for U.S. installations. You should consider the working space required for technicians and operators including access to the rear of the game.

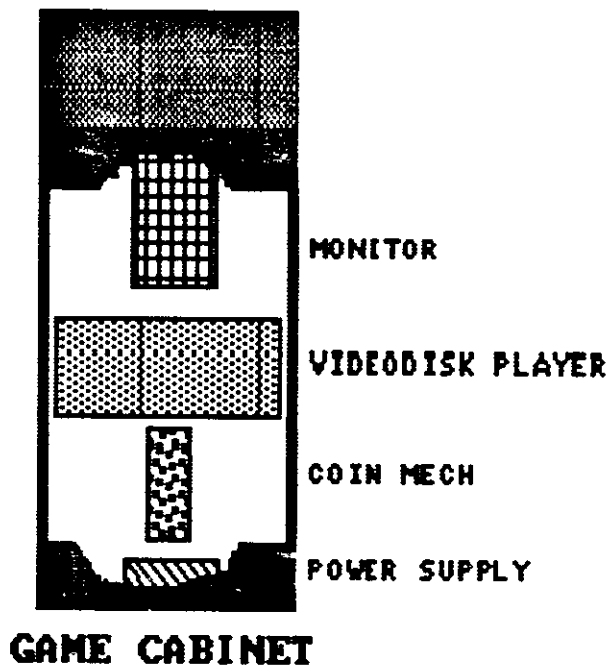
NOTE: The cabinet must be within five (5) feet of an AC outlet. Be certain that a grounding (3 wire) outlet is available.

**CAUTION: DO NOT** remove the AC ground prong from the plug as this creates a serious safety hazard. Doing so VOIDS your warranty.

5. MAJOR COMPONENTS

The FREEDOM FIGHTER™ game is a colorfully illustrated video game with high resolution digital and laser disk graphics. The major components of your game are illustrated in Fig. 1 and include the following:

- \* Control Panel & controls
- \* Coin mechanism
- \* Monitor
- \* Power Supply Assembly
- \* Speakers
- \* Laser Disk Player
- \* All PCB assemblies
  - ..... \* Game Logic PCB
  - ..... \* Digital Audio PCB
  - ..... \* Video Expander PCB



II. ADJUSTMENTS

1. POWER SUPPLY INFORMATION AND ADJUSTMENTS

All DC Power required to operate the FREEDOM FIGHTER™ is supplied by the MILLENNIUM GAMES PRODUCTS Power Supply Module. These supply outputs are as follows:

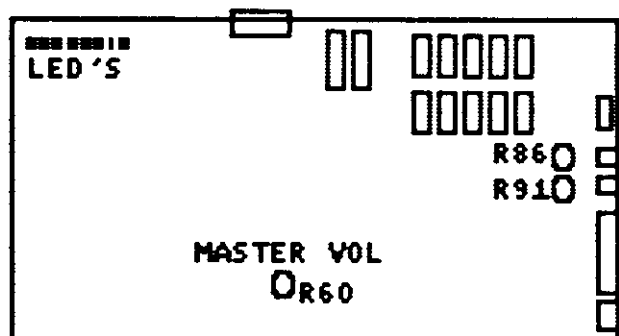
- \* +5 VDC @ 11 amps
- \* +12 VDC @ .5 amps
- \* +18 VDC @ 2 amps
- \* -18 VDC @ 2 amps

**CAUTION:** Only certified technicians should make these adjustments. Only the +5 VDC is adjustable and should be measured at the terminal block and set to +5.07 +/- .03 VDC.

2. AUDIO PCB ADJUSTMENTS

The FREEDOM FIGHTER™ game is presently set up for monaural sound both digitally and from the disk player. To provide a balanced mix of digital and disk player sounds:

1. Adjust master audio volume control R60 located at position 6M for digital volume level. Use the shoot sound during game play.
2. Adjust disk player audio volume controls R86 & R91 at location A4 for disk volume level adjusting both pots equally. The audio level should equal the digital sounds.





3. OPERATOR SELECTABLE GAME OPTIONS

This menu is selected through the manual diagnostics menu. To access the manual diagnostics, the game must be in the attract mode. At this point you press the test button located inside the coin door and the following Menu appears.

```

Test Logic Eproms
Test Ram
Test Interrupts
Test DMA
Test Disk Player
Test Video Expander
Test Internal Video
Test Internal Color
Test Sound Board
Reset High Scores
Reset Game Options
Exit
    
```

To pick the game options move the pointer with the joystick control to the - Reset Game Options - and pull the trigger button to activate the next menu. The recommended settings are listed as bold, underlined characters below.

- \* SloMo Enable ..... (ON) (off)  
This either enables slow motion (on) or disables slow motion (off) when slomo button is pressed.
- \* SloMo Speed [fraction of normal speed] ..... (.5) (.66) (.75) (.80)  
This sets the speed of slow motion in relation to normal speed (i.e. - .5 is 50% of normal speed).
- \* Max SloMo Time/game in sec. .... (8) (6) (4) (2) (0)  
The amount of slow motion time is limited in each game. The maximum amount is set here. Setting 0 is the same as disabling slow motion.
- \* Target Size [Game Difficulty] ..... (2X) (1.5X) (1.25X) (normal)  
This sets the size of the target area to shoot. The bigger the target, the easier it is to hit, therefore setting the game difficulty.
- \* Number of Lives ..... (6) (5) (4) (3)  
This sets the total number of lives for one game.
- \* Number of coins per credit ..... (1) (2) (3) (4) (5) (6)  
This sets the number of quarters per game credit. (i.e. 2 = \$.50 game)
- \* Number of extra lives on prog coin drop ... (no prog coin) (1) (2)  
Progressive coin drop enables the player to continue play starting at the previous finish point for another credit.
- \* Progressive lives to train station or ALL ..... (TRAIN) (ALL)  
This enables extra lives on a progressive coin drop for anywhere in the game if you choose (all) or enables extra lives only to the train station if you choose (train) provided (no prog coin) was NOT chosen in the previous selection.
- \* Attract mode sound ..... (Yes) (No)  
This enables (yes) or disables (nc) sounds during the attract mode.

4. VIDEODISK ASSEMBLY

a. Parts

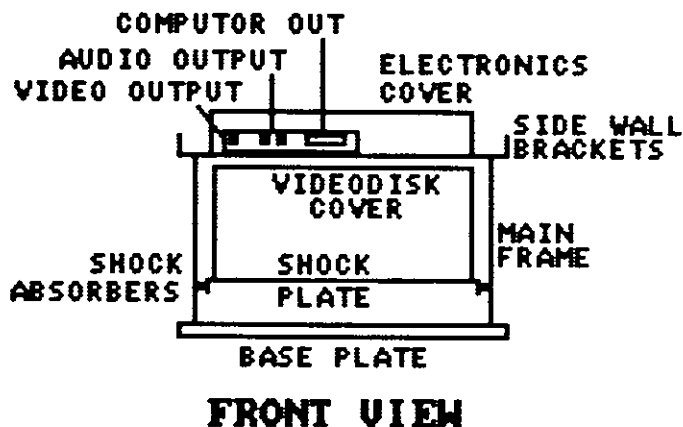
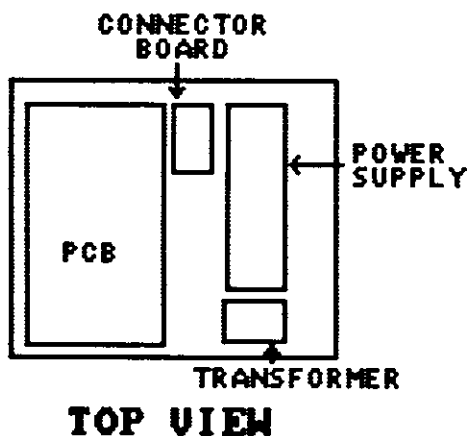
1. Main Frame
2. Shock Plate
3. Shock Absorbers
4. Electronics Cover
5. Videodisk Drive
6. Videodisk Drive Cover
7. PC Electronics and Video Boards
8. Power Supply
9. Transformer
10. Connector Board
11. Ribbon Cable
12. Video Cable
13. Power Cable

b. Removing Videodisk Player Assembly from cabinet

Disconnect all computer, video, audio and power cables. Unscrew side wall brackets (see fig 3), slide Videodisk assembly out.

c. Troubleshooting

Select "Disk Player" from the Manual Diagnostics Menu, pull the trigger to play through test scenes, color bars and centering diagrams. If first test scene does not come up or pulling the joystick trigger does not advance the test scene sequence, the videodisk player has a problem. Check to see that all power, computer, video and audio cables are securely fastened. Try test sequence again. If the player still fails to respond, call the customer service line. UNDER NO CIRCUMSTANCES REMOVE THE ELECTRONICS COVER OR THE VIDEODISK ASSEMBLY COVER.



## III. MODES OF OPERATION

## 1. AUTO DIAGNOSTICS MODE AND STARTUP

## a. STARTUP

The game may be started by switching on the power switch located toward the rear on the lower right hand side of the cabinet. The game screen will appear in approximately one to two minutes if all systems check OK. The auto diagnostics mode occurs automatically at power up. These tests are generally the same tests that can be performed in the manual diagnostics mode. No message is displayed if everything is OK. If an error is found, an error code is displayed on the LED display located on the main logic PCB. Error codes are listed in the error code listing. If the screen does not appear after two minutes an error may have been detected. Check the LED display for the code. If necessary, these power-up tests can be skipped to permit game operation by holding the trigger down before turning on the power switch and by continuing to hold the trigger down until the game screen appears. Of course, if a significant hardware problem exists, the game screen may not appear and then power-up diagnostics procedures should be followed.

The joystick is self-adjusting and should be turned all the way right, left, up and down a few times after power-up to ensure accuracy.

## b. POWER-UP DIAGNOSTICS

Each time game cabinet power is switched on, a series of diagnostic tests are performed to check the game hardware. If no errors are detected, power-up continues until the game goes into the attract mode. This usually takes one to two minutes. If an error is detected however, power-up will halt and a number indicating the error found is shown on the main logic board LED display. In this case, the operator or service person should open the rear cabinet door and write down the pattern of lights shown on the LED display on the main logic board. This pattern can be decoded and referenced as described in the Error Code Listing section. After noting the error message pattern shown on the LED display, the operator should return to the front of the cabinet and hold the game trigger down for a second or so to permit continued power-up. If an additional error is detected, power-up will again be halted and the procedure given above should be repeated. It may be necessary to repeat these steps a number of times before the attract mode screen appears, noting the error message patterns on the LED display for each occurrence.

## 2. MANUAL DIAGNOSTICS MODE

To access the manual diagnostics, the game must be in the attract mode. Press the test button located inside the coin door and the following Menu will appear:

```

Test Logic Eproms
Test Ram
Test Interrupts
Test DMA
Test Disk Player
Test Video Expander
Test Internal Video
Test Internal Color
Test Sound Board
Reset High Scores
Reset Game Options
Exit

```

To pick one of the tests move the pointer with the joystick control and pull the trigger button to activate the test. The tests are described below in more detail.

## a. TEST LOGIC EPROMS

This tests the game eproms on the main logic PCB located in rows 1 thru 11 in columns A and C. If an error is detected, a message indicating the problem eprom pair is shown on the screen. In this case, pull the trigger briefly to continue. If no errors are found, the menu screen will reappear after one or two seconds and no error will be shown.

## b. TEST LOGIC RAM

This selection tests the moving object ram and the screen ram. If an error is detected, a message will indicate the problem ram. Otherwise, the menu screen will reappear after approximately 5 seconds.

## c. TEST INTERRUPTS

This tests the video interrupt and the joystick interrupts. If an error is detected a message will indicate the error, otherwise the menu screen will immediately reappear.

## d. TEST DMA

The DMA chip (68440 at 28-C) is tested by this routine. If no error is found, the menu screen will reappear. A moving object problem may indicate a DMA when in fact the DMA is OK.

## e. TEST DISK PLAYER

Tests disk player by first going to (5) five game scenes, then advances to a crosshatch pattern. It then goes to a full screen color bar test and to a smaller color bar test. To advance thru the frames, pull the trigger. After the last frame, the menu screen will reappear.

## f. TEST VIDEO EXPANDER

This puts the screen into an expanded mode. Turn joystick full left and full right to see the full expanded screen. When this test is run without leaving manual diagnostics, all other tests will also be in expanded video mode. Pull the trigger button to return to the menu screen.

## g. TEST INTERNAL VIDEO(DIGITAL)

When this selection is made, eight pairs of vertical color bars appear against a black background, representing the sixteen colors in the background digital graphics palette. After a few seconds, 64 moving objects containing the sixteen colors will appear over the background bars so that any problems in the graphics color and priority table hardware can be observed. The lower right moving object should make a counter-clockwise circuit of the screen to demonstrate that the moving object control is OK. After the moving object has returned to the lower right position, pull the trigger to return to the menu screen.

## h. TEST INTERNAL COLOR(DIGITAL)

This selection brings up a screen for testing and setting monitor color and overscan adjustments. It consists of four columns of color blocks, with seven blocks in each column. The lefthand column is red, the next is green, the next blue, and the righthand column is white. The top blocks in each column have a very low saturation of the colors, and saturation increases equally for all colors on each vertical row down, until full saturation is reached in the bottom row. The entire block pattern is surrounded by four lines drawn in rectangles at the border of the screen. The outermost is red and appears 8 pixels inside the edge of the computer defined screen. Inside that are green, blue, and white rectangles each 4 pixels inside the other. All rectangles are drawn in low color saturation. The top blocks in each column should be adjusted so that they are barely visible. Pull the trigger to return to the menu screen.

## i. TEST SOUND BOARD

This selection tests the sound board via the communication port from the main board. If no communication can be established with the sound board this will be indicated and other sound error messages can be disregarded. Lack of communication with the sound board can be caused by lack of power to the sound board, by a bad ram chip on the sound board (2A), by a bad sound control chip (1A), or by a problem with the communication cable. If no communication problem is indicated, any errors in the ram or eproms will be displayed, along with their location. If no errors are detected, the menu screen will reappear in a few seconds.

## j. RESET HIGH SCORE TABLE

This selection resets all initials to blanks and high scores to zero in the high scores screen shown in the attract mode. The process takes about 10 seconds, after which the menu screen reappears.

## k. RESET GAME OPTIONS

Allows operator to reset game options. These options are explained in II. ADJUSTMENTS, 3. OPERATOR SELECTABLE OPTIONS.

## l. EXIT

This selection causes the power-up process to restart and returns game to the Attract Mode.

### 3. ATTRACT MODE

The attract mode appears after powerup auto diagnostics and after every game. This mode will continue to display the attract mode repeatedly until the proper amount of coins are deposited, and the trigger button is pressed. Depending on the option selected, there may or may not be sound during the attract mode.

### 4. GAME PLAY MODE

Your mission is to fight through the city and take over the train. From there you progress to the planet of the evil guardian. It is then your mission to defeat the evil guardian. The instructions for play are as follows:

- \* To choose the direction of travel or jump out of the way of oncoming threats, turn joystick to the left or right.
- \* Aim your laser pistol by positioning the cursor over the intended target.
- \* Fire your laser pistol by pulling the trigger.
- \* Action may be slowed down by pushing the "SLO-MO" buttons located left and right of the joystick. There is a limited amount of "SLO-MO" during each game. Use it wisely.
- \* If you are killed and have lives remaining, game returns to the previous path decision point and starts again.

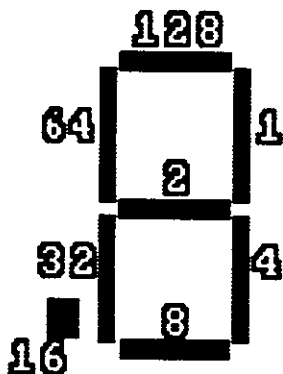
### In-Game Error Detection

In addition to the power-up diagnostics, features have been built into the game that permit it to detect minor hardware errors yet permit continued normal game operation. If such an error is detected in the course of the game, error lights will be lit on the main board LEDs, (See Error Code Listing On Next Page).

IV. ERROR CODE LISTING

1. Error Messages

The main game board contains a 7 Segment LED with decimal point that is used to show errors detected upon power-up or during game operation. The 8 leds represent 8 bits of a binary error message number. It is interpreted by adding the number represented by each LED that's ON. NOTE: All LEDs OFF indicate no error.



For example, if leds 1,16, and 32 were ON, this would be indicating error number 49, (1+16+32=49). If leds 2,4,8, and 64 were ON, error 78 would be indicated. (2+4+8+64=78).

Error messages are shown below.

Error #	Message
1	Error in logic board eprom pair 10/11A &/or 10/11C
2	Error in logic board eprom pair 9A &/or 9C
3	Error in logic board eprom pair 8A &/or 8C
4	Error in logic board eprom pair 7A &/or 7C
5	Bad system ram
6	Bad moving object ram
7	Bad screen ram
8	DMA error
9	A to D interrupt error
10	Video vertical interrupt error
11	Timer interrupt error
12	Video disk player not responding
13	No video disk player initialization
14	Error in main game control logic eproms 4-5/A &/or 4-5/C
15	Unidentified video disk error
16	Invalid video disk read
17	No video disk raster pulse
18	Multiple video disk raster pulses missing
19	Video disk GOTO timeout
20	Invalid video disk control command
21	Incomplete video disk comand
22	No sound board communication
23	No sound board communication
24	Sound board ram error - 2A
25	Sound control eprom error - 1A
26	Sound eprom error - 1FG
27	Sound eprom error - 1E
28	Sound eprom error - 1D

2/2/82

- 29 Sound eprom error - 1BC
- 30 Sound eprom error - 2FG
- 31 Sound eprom error - 2E
- 32 Sound eprom error - 2D
- 33 Sound eprom error - 2BC
- ref 2/6* 34 Bus error accessing system ram (0 - 3FFF)
- 35 Bus error accessing I/O (4000 - 402F)
- 36 Bus error accessing A to D conversion hardware (4030 - 05F)
- 37 Bus error accessing LED (4060 - 406F)
- 38 Bus error accessing unassigned address space (4070 - 7FFF)
- 39 Bus error accessing moving object ram (8000 - FFFF)
- 40 Bus error accessing video lookup tables (10000 - 107FF)
- 41 Bus error accessing unassigned address space (10800 - 13FFF)
- 42 Bus error accessing DMA (14000 - 140FF)
- 43 Bus error accessing unassigned address space (14100 - 1BFFF)
- 44 Bus error accessing E square storage chip (1C000 - 1C3FF)
- 45 Bus error accessing unassigned address space (1C400 - 100000)
- 46 Bus error accessing video chip (100001 - 1000FF)
- 47 Bus error accessing unassigned address space (100100 - 1BFFFF)
- 48 Bus error accessing screen ram (1C0000 - 1DFFFF)
- 49 Bus error accessing unassigned address space (1E0000 - 1FFFFFF)
- 50 Bus error accessing logic board eproms (200000 - 25FFFF)
- 51 Bus error accessing unassigned address space (260000 - FFFFFFFF)
- 52 Address error accessing system ram (0 - 3FFF)
- 53 Address error accessing I/O (4000 - 402F)
- 54 Address error accessing A to D conversion hardware (4030 - 405F)
- 55 Address error accessing LED (4060 - 406F)
- 56 Address error accessing unassigned address space (4070 - 7FFF)
- 57 Address error accessing moving object ram (8000 - FFFF)
- 58 Address error accessing video lookup tables (10000 - 107FF)
- 59 Address error accessing unassigned address space (10800 - 13FFF)
- 60 Address error accessing DMA (14000 - 140FF)
- 61 Address error accessing unassigned address space (14100 - 1BFFF)
- 62 Address error accessing E square storage chip (1C000 - 1C3FF)
- 63 Address err accessing unassigned address space (1C400 - 100000)
- 64 Address error accessing video chip (100001 - 1000FF)
- 65 Address err accessing unassigned address space (100100 - 1BFFFF)
- 66 Address error accessing screen ram (1C0000 - 1DFFFF)
- 67 Address err accessing unassigned address space (1E0000 - 1FFFFFF)
- 68 Address error accessing logic board eproms (200000 - 25FFFF)
- 69 Address err accessing unassigned address space (260000 - FFFFFFFF)
- 70 Illegal instruction error
- 71 Divide by zero error
- 72 Chk instruction
- 73 Trapv instruction
- 74 Privilege violation
- 75 Trace
- 76 Op code 1010
- 77 Op code 1111
- 78 Unexpected trap encountered
- 79 Unused
- 2/24/82* 80 No video disk interrupt
- 81 Video disk Davnot line inactive
- 82 Video disk busy line not responding
- 83 Error in Table Driven Game Logic



## GENERAL OVERVIEW

The hardware is composed of eight (8) separate subsystems and when connected together, they form an integrated game system. The different subsystems are as follows:

### 1. POWER SUPPLY ASS'Y

The power supply ass'y supplies the necessary voltages required by the different subsystems of the game.

The input voltage is: 115V/220V AC 60 HZ AT 5 AMPS MAX.

The output voltages are: 115 VAC for the fan and logo lamps  
115 VAC isolated @ 1.5 Amps for monitor  
+18 VDC @ 3 Amps; -18 VDC @ 3 Amps; +5 VDC @ 10 Amps

### 2. COLOR MONITOR ASS'Y

The color monitor is a standard raster display monitor with a horizontal frequency of 15.75 khz and a vertical refresh of 60 hz. The color input is analog RGB at 2 Volts peak to peak. The sync input is TTL with separate horizontal and vertical drives.

### 3. VIDEO DISK PLAYER

The video disk player is a ruggedized version of a commercial player and provides the animated video for the game. Standard NTSC composite video is output by the player. The main logic pcb provides the control of the output video by determining on a frame by frame basis which video to output.

### 4. MAIN LOGIC PCB

The main logic pcb contains the game program and functions to control the other subsystems in the game. This pcb is responsible for the generation of digital video, accepting player inputs, controlling the disk player, controlling the video expander pcb, and controlling the audio pcb. The main logic also contains the output drivers for the color monitor.

### 5. VIDEO EXPANDER PCB

The video expander pcb converts the analog RGB signals from the NTSC pcb to 5 bit digital information, which allows the digital expansion of video data.

### 6. NTSC TO RGB CONVERTER

The NTSC to RGB converter pcb converts the composite video signal from the disk player to individual analog signals -- Red, Green, and Blue to be used in the video expander pcb.

### 7. AUDIO PCB

The audio pcb generates all transit or player generated sounds for the game. This pcb also contains the audio power amplifier to drive the two speakers. In addition, external inputs to the pcb allow audio generated by the disk player to be amplified by the power amplifier.

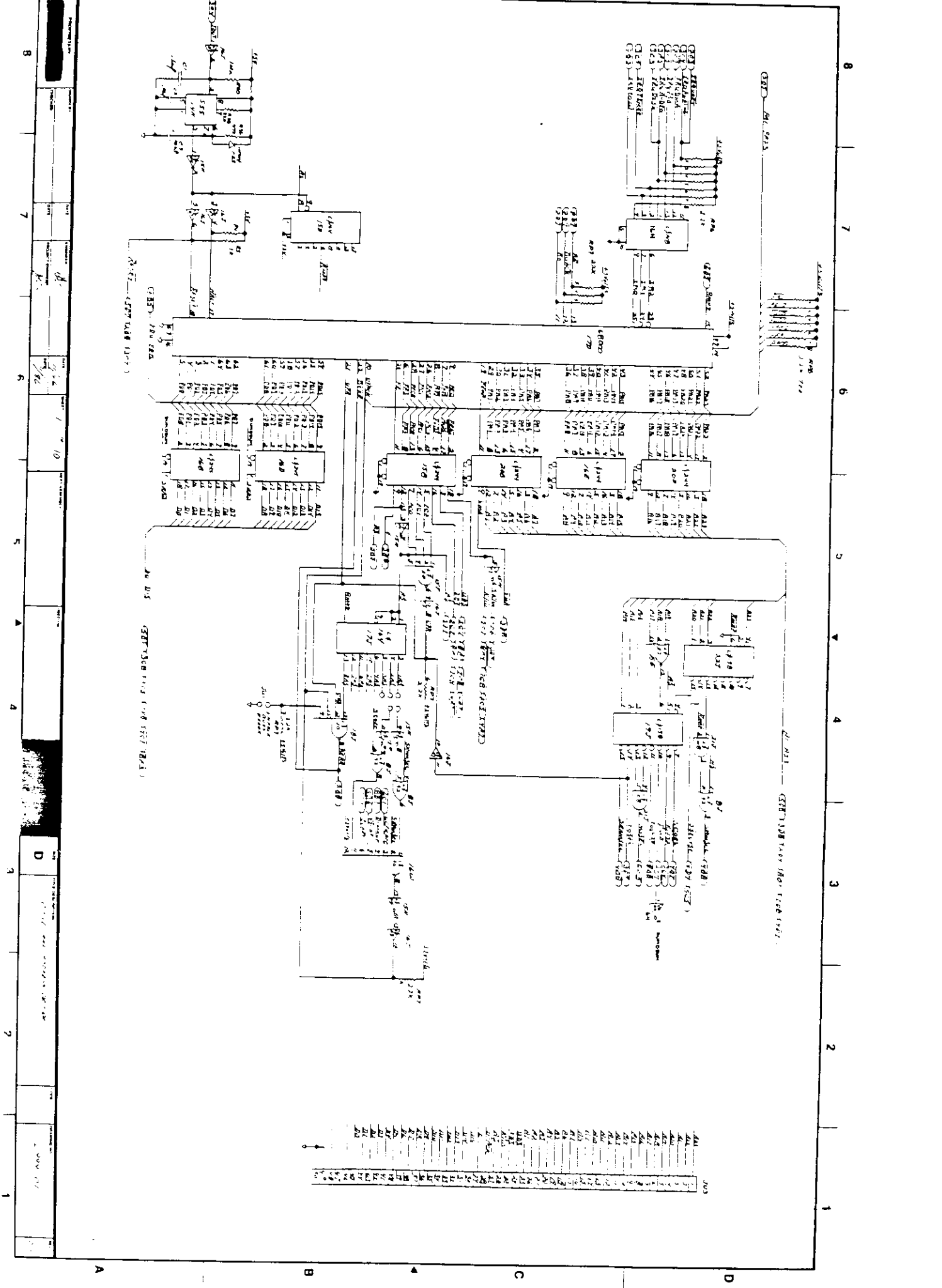
### 8. CONTROL PANEL ASS'Y

The control panel is the interface between the player and the game. Player movement is controlled by the joystick, and weapons are fired by the joystick trigger. Game speed can also be controlled by the player by using the slow motion button.

## CPU AND ADDRESS DECODING LOGIC SCHEMATIC PAGE 1 of 10

Schematic Grid Location	Board Location	Function
D7	16H	Interrupt priority encoder
C6	17D	CPU
C5,D5	20P,16E,20B	Address line buffers
B5	15B	Control line buffer
B5	16D,16B	Data line buffers
A8	14H	Power on reset ckt
B7	15D	Power on reset remap of ROM
-	-	memory space to pick up stack
-	-	pointer and reset vector
B4	17J	DTACK delay circuit
B3	16W	DTACK combination circuit

This page contains the heart of the game system. The CPU implemented in this system is the MC68000 (17D). The CPU address lines are buffered by three (3) 74LS244s (20P,16E,20B), and then distributed throughout the main logic pcb. System address decoding is performed by two (2) 74LS138s (22J,19J), and these enable signals are used by each major system on the board to control the transfer of data. Data line buffering is the function of the two (2) 74LS245 (16B,16D). CPU control line buffering is performed by the 74LS244 (15B). Power on reset is accomplished by the NE555 (14H) and the 74LS164 (15D). CPU interrupts are applied to the processor through a priority encoder 74LS148 (16H). The circuitry of the 74LS164 (17J), 74LS30 (16W), and 74LS20 (18J) provide the necessary signals to accept DTACK responses from each major system on the board and to generate buss error conditions encountered by the CPU. JU3 is an expansion connector, which is not used in this implementation of the game system. This connector is for future expansion.



NO.	DESCRIPTION	QTY	UNIT	REMARKS
1	7410	1	IC	
2	7411	1	IC	
3	7412	1	IC	
4	7413	1	IC	
5	7414	1	IC	
6	7415	1	IC	
7	7416	1	IC	
8	7417	1	IC	
9	7418	1	IC	
10	7419	1	IC	
11	7420	1	IC	
12	7421	1	IC	
13	7422	1	IC	
14	7423	1	IC	
15	7424	1	IC	
16	7425	1	IC	
17	7426	1	IC	
18	7427	1	IC	
19	7428	1	IC	
20	7429	1	IC	
21	7430	1	IC	
22	7431	1	IC	
23	7432	1	IC	
24	7433	1	IC	
25	7434	1	IC	
26	7435	1	IC	
27	7436	1	IC	
28	7437	1	IC	
29	7438	1	IC	
30	7439	1	IC	
31	7440	1	IC	
32	7441	1	IC	
33	7442	1	IC	
34	7443	1	IC	
35	7444	1	IC	
36	7445	1	IC	
37	7446	1	IC	
38	7447	1	IC	
39	7448	1	IC	
40	7449	1	IC	
41	7450	1	IC	
42	7451	1	IC	
43	7452	1	IC	
44	7453	1	IC	
45	7454	1	IC	
46	7455	1	IC	
47	7456	1	IC	
48	7457	1	IC	
49	7458	1	IC	
50	7459	1	IC	
51	7460	1	IC	
52	7461	1	IC	
53	7462	1	IC	
54	7463	1	IC	
55	7464	1	IC	
56	7465	1	IC	
57	7466	1	IC	
58	7467	1	IC	
59	7468	1	IC	
60	7469	1	IC	
61	7470	1	IC	
62	7471	1	IC	
63	7472	1	IC	
64	7473	1	IC	
65	7474	1	IC	
66	7475	1	IC	
67	7476	1	IC	
68	7477	1	IC	
69	7478	1	IC	
70	7479	1	IC	
71	7480	1	IC	
72	7481	1	IC	
73	7482	1	IC	
74	7483	1	IC	
75	7484	1	IC	
76	7485	1	IC	
77	7486	1	IC	
78	7487	1	IC	
79	7488	1	IC	
80	7489	1	IC	
81	7490	1	IC	
82	7491	1	IC	
83	7492	1	IC	
84	7493	1	IC	
85	7494	1	IC	
86	7495	1	IC	
87	7496	1	IC	
88	7497	1	IC	
89	7498	1	IC	
90	7499	1	IC	
91	7500	1	IC	

## DMA AND SERIAL I/O SCHEMATIC PAGE 2 of 10

Schematic Grid Location	Board Location	Function
C7	21D	DMA device
D6	20H	Address line buffer for DMA
C6	19D	Address line buffer for DMA
B6	19H	Data line buffer for DMA
B6	19B	Data line buffer for DMA
C4	11J (opt.)	Data line buffer for serial
C4	12J (opt.)	2 channel serial driver
C3	1J (opt.)	TTL to RS232 driver
C3	14J (opt.)	RS232 to TTL driver

Memory to memory transfers are performed by the Direct Memory Access device MC68440 (21D). This DMA device is programmed by the CPU to move data from ROM to other parts of the system.

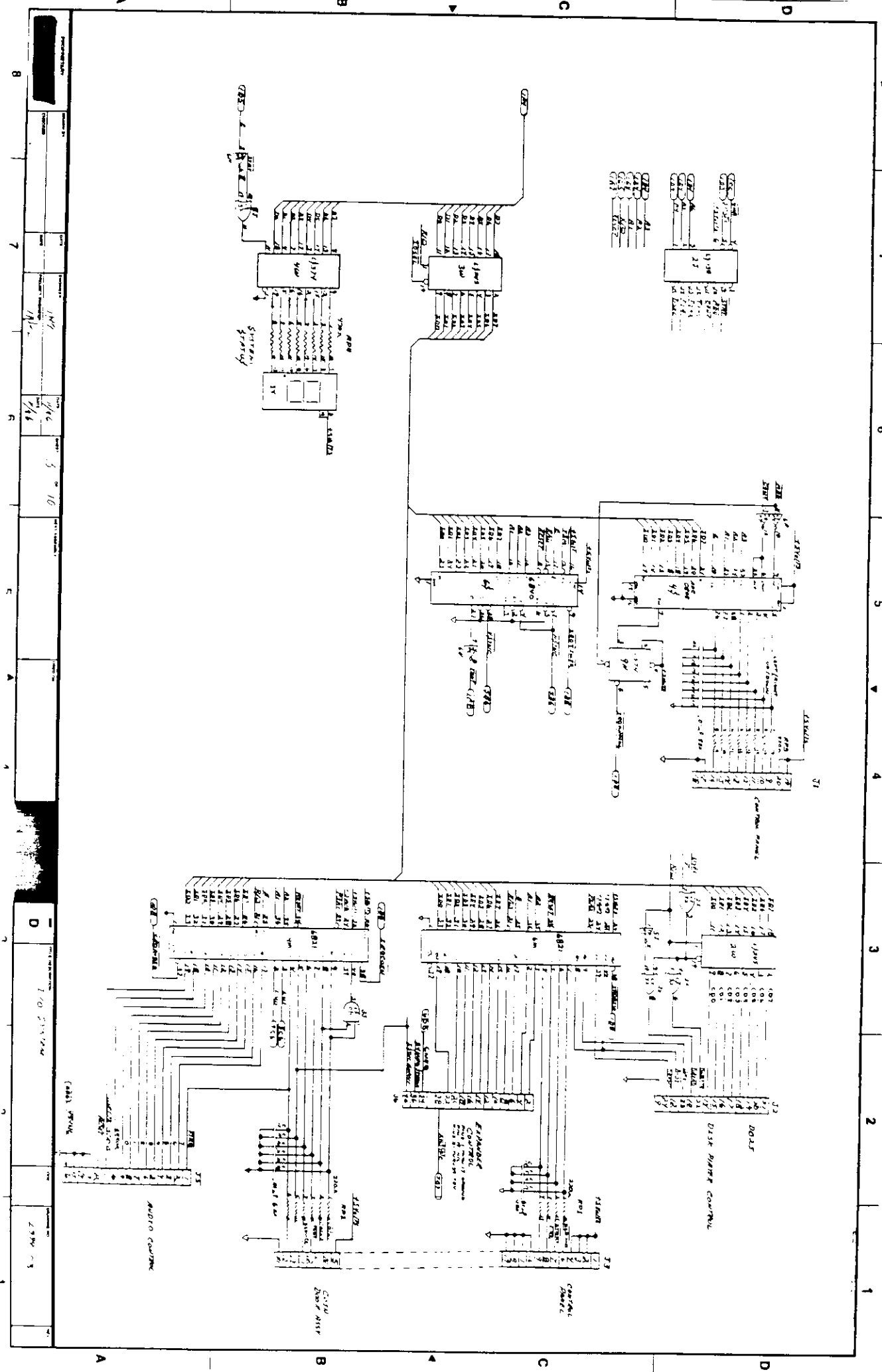
Designed for future applications, a two channel serial input and output device, the MC68681 (12J) is included in the system. The components required for this function were intentionally not installed into this pcb.



## I/O SYSTEM SCHEMATIC PAGE 3 of 10

Schematic Grid Location	Board Location	Function
D7	2J	I/O address decoder
C7	3W	I/O data line buffer
B7	4W	System status output driver
B6		Error code display
D5	4S	Analog to digital converter
C5	9H	Interrupt driver for converter
C5	6S	3 channel timer
D3	2W	Video disk data line buffer
C3	6M	Disk, control panel, Expander I/O
B3	4M	Coin door and Audio I/O

The Address lines are decoded by the 74LS138 (2J), and device enables are generated to select each device on this page of the system diagram. The analog to digital converter ADC0808 (4S) converts the movement of the joystick to digital signals. The two inputs presently being used are pins 9 and 10 of connector J1. This device generates interrupts to the CPU through the 74LS74 (9H) when a conversion is complete. The video disk interface circuitry through connector J2, performs all command and communication with the video disk. Connector J3 connects the control panel and coin door to the system. These signals are conditioned by passive components and are applied to the two MC6821s (6M) (4M). The interface between the video expander and the main logic pcb is accomplished through the MC6821 (6M). This interface controls the operation of the expander. Expander enable is generated from pin 19 of the MC6821 while the other pins control the display start position of the expanded line. Several other signals are required to interface the expander pcb. These are timing and enable signals. Communication and control of the audio pcb is accomplished through connector J5.



PROJECT TITLE		DATE		DRAWN BY		CHECKED BY	
CONTROL BOARD		1/10/68		J.M.C.		J.M.C.	
SHEET NO.		REV.		SCALE		SHEET TOTAL	
1		0		1/16"		10	
PROJECT NO.		REV.		DATE		BY	
100-200000		0		1/10/68		J.M.C.	

CONTROL BOARD  
 DISK DRIVE CONTROL  
 AUDIO CONTROL  
 SYSTEM STATUS  
 CIRCUIT BREAKER

FREEDOM FIGHTER MANUAL

ROM, RAM, AND CORE SCHEMATIC PAGE 4 of 10

Schematic Grid Location	Board Location	Function
C6	12B	Data line buffer to ROM
B6	13D	Data line buffer to ROM
D5,D4	2A,3A,4A,6A,7A,8A,9A,10A	Program and Data ROM
C5,C4	2C,3C,4C,6C,7C,8C,9C,10C	Program and Data ROM
D3	2E	System RAM
C3	3E	System RAM
C3	5E	Electrical Erasable ROM
A5	7H	ROM address decoder
A7	15J	Write control to system RAM
B7	6J	ROM data buss enable decoder

The system ROM and RAM are contained on this page of the system diagram. The address decoding for the selection of individual components are accomplished by the 74LS138 (7H). Selection jumpers JU7, JU6, and JU5 are used if 27512 Eproms are installed into the system.





## BACKGROUND VIDEO GENERATOR SCHEMATIC PAGE 5 of 10

Schematic Grid Location	Board Location	Function
C6	12Z	Video Controller Device
D5	14X	Video RAM Counter
D4	12R	Video RAM decoder
C5,C4,C3,C2	11W,10W,13W,12W	Video RAM
C4	14S	Video data line buffer
C3	14W	Video data line buffer
B6	15X	External sync buffer
A5	11R	Horz line resync counter
A5	12R	Resync decoder

The background digital video is comprised of the TMS32061 (12Z). This device controls the video display and dynamic memory PD41264s (11W,10W,13W,12W). External synchronization is accomplished through the circuitry of the 74LS374 (15X).



## CLOCK AND MICROCODE SCHEMATIC PAGE 6 of 10

Schematic Grid Location	Board Location	Function
D7	9L (opt.)	Internal clock generator
D6	11M,11M,10J	Divide by 3 ckt
C6	10J,10L,10L	Divide by 2 and divide by 2
C7,C6	external pcb	Resync logic to disk pcb
C4	12M	Microcode jump select
C3	13L	Microcode program counter
C3	14M,13M	Microcode program PROM
C1	14R	Microcode control driver

The generation of the various clocks required for the system are accomplished through the circuitry of 11M, 10J, and 10L. The input clock to this circuitry can be internally generated or externally generated - as it is with a disk player. The control of the dynamic digital moving objects is through the microcode sequencer, composed of 11L,12M,13L,14M,13M,12L, and 14R. This sequencer controls the addressing and enabling of data transfers of the circuitry, on page 7.



## HIGH SPEED OBJECTS SCHEMATIC PAGE 7 of 10

Schematic Grid Location	Board Location	Function
C8	22M	R/W control to object RAM
D7	13R	CPU address controlled driver
C7	21R	CPU address controlled driver
C7	15M	Next object address counter
B7	20M	Object address pointer reg
B7	20S	Object address pointer reg
D6,C6,B6	18S,18M,19M,19S	Object list and data RAMs
A6	21S	Vert line counter for active
A6	21W,20W	Adder for active line select
B5	22S	Active Object this line cont
D6,C6,B6	16S,17S,16M,17M	Object data line buffers
D5,C5,B5	15K,17L,19L,21L	Object image data buffers
D5,C5,B5	16L,18L,20L,22L	Object image shift reg
D4	18W,20S	Object Horz position reg
C4	22X	Odd line serial image buffer
B4	22X	Even line serial image buffer
D3	17Z,18Z,19Z	Object odd line horz position
C3	17Y,18Y,19Y	Object even line horz position
D2	20Z	Object odd line RAM
B2	20Y	Object even line RAM
C2	21Y	Active line output multiplexer
B2	20J	Odd and even line control
A2	16Z	Object load and shift control
A3	21Z	Odd even line control flip flop

The RAMs 6264(18S,18M,19M,19S) are the central point of the digital moving object system. The CPU and/or DMA device can access this RAM to read, write, and modify the data. The RAM is logically set up into different parts, which are: 1. Moving object display list 2. Moving object display data. The moving object display list defines the x/y location for the object and a pointer to the address within the RAM where the definition of the object is found. The microcode sequencer on page 6, controls the operation and transfers of data within this page. The overall sequence of operation is as follows:

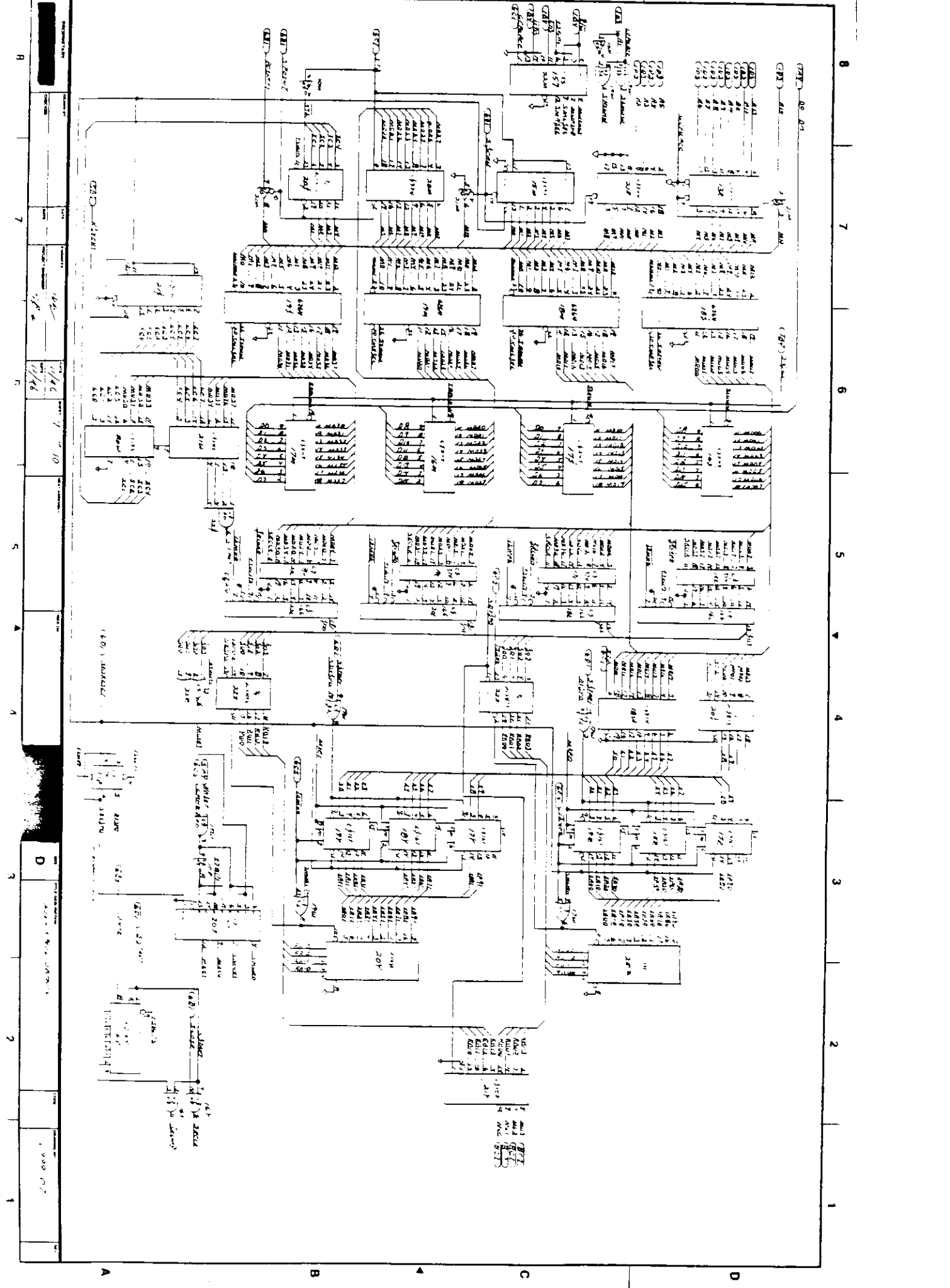
1. The display list is scanned sequentially by counter 15M. If, by a comparison of the current display line and the y position of the object (21S,21W,20W) it is found that the object should be visible (22S), then the line number of the object that is to be displayed, is stored in 20S. At the same time, the base address of the object is stored in 20M. Therefore, at this point in the sequence it has been determined that an object should be displayed, and its address is stored in registers.

2. The line number to be displayed of the object is added to the base address of the object, which forms an address to the RAM from where the data is to be retrieved. Data is retrieved in four 8 bit bytes which are the first, or left side, of the 16X16 object and are stored in registers 15K,17L,19L, and 21L.

3. The right side of the object is now addressed by adding a logic 1 to the previous address (20M,20S). This data is now stored in registers 15K,17L,19L, and 21L as in the previous step, but the data that was stored in these registers is transferred to the serial shift registers 16L,18L,20L, and 22L.

4. The object data is converted from parallel to serial and is applied to either the odd or even line buffer RAM (20Z or 20Y). This odd and even line buffer allows one line to be written to, while the other line is read from, resulting in a high speed buffer system. The address, the data is written into, is derived from the horizontal position registers 17Z,18Z,19Z and 17Y,18Y,19Y. Once the first eight pixels of four bits each is shifted into the RAM, the next or right side data, is transferred to the shift registers and the operation continues.

5. When the shift is complete for the right side data, the microcode accesses the RAM for the next entry in the display list. If an entry is not to be displayed, that entry is skipped and the operation continues to the next entry.



8 7 6 5 4 3 2 1

A B C D

PROJECT TITLE	DATE	SCALE	DESIGNER	CHECKER
REVISIONS	NO.	DATE	BY	REASON



## VIDEO LOOKUP AND OUTPUT SCHEMATIC PAGE 8 of 10

Schematic Grid Location	Board Location	Function
D7		+12 volt power for video out
B7	9J	Lookup table access control
C5	8S	Serial Video combiner buffer
C5	8L	Lookup R/W control multiplexer
B5	10R	Lookup address buffer
C5,B5	7M,8M,9M,10M	Lookup table RAM
D4	8Z,8X	Digital video input from disk
C4	9J	Digital video enable
C4,D4	7S,7R	Internal digital video buffer
B4,A4	7R,9R	Lookup table data line buffer
B3,C3	5X,6X,7X	Digital video level converter
D2	Q2,Q1	Red digital to analog driver
C2	Q4,Q3	Green digital to analog driver
B2	Q6,Q5	Blue digital to analog driver
B2	Q7	D to A bias and blanking
A2	3X	Sync output Polarity

This page contains the VIDEO LOOKUP TABLE AND VIDEO OUTPUT DRIVERS. High speed moving object data is combined with background video data to form an 8 bit address to the lookup table (8S). The data at this address is the color information that should be displayed on the crt. The color information (in the form of 5 bits for each color: red, blue, and green) is placed in the lookup table by the CPU through address buffer (10R) and data buffers (7R) and (9R). Control of this data read and write operation is performed by (8L). Connector J8 is the external digital video input which accepts the output from the video expander pcb. This digital input is enabled by bit 15 of the lookup table through (9J) being a logic "0". The video output stages are a form of digital to analog converter which converts a weighted current amount, depending on the position of the active bit, into a voltage. This voltage swing is from approximately .8 volts to 3.5 volts.



## VIDEO EXPANDER SCHEMATIC PAGE 9 of 10

Schematic Grid Location	Board Location	Function
C7	A3,D3	Digital video buffer odd line
B7	A4,D4	Digital video buffer even line
A7	B9	External sync enable
D6	B8,B7,B6	Odd line address counter
B6	C8,C7,C6	Even line address counter
A6	D9	Odd or even line flip flop
A5	D8	Line reset and start control
A4	D9	Output clock generation
D4	B5,B4,B3,B2	Odd video line RAM
B4	C5,C4,C3,C2	Even video line RAM
D3	A6,D6	Odd line output buffer
B3	A5,D5	Even line output buffer
A3	D7	Odd even RAM R/W control
B1	-	External resync pcb

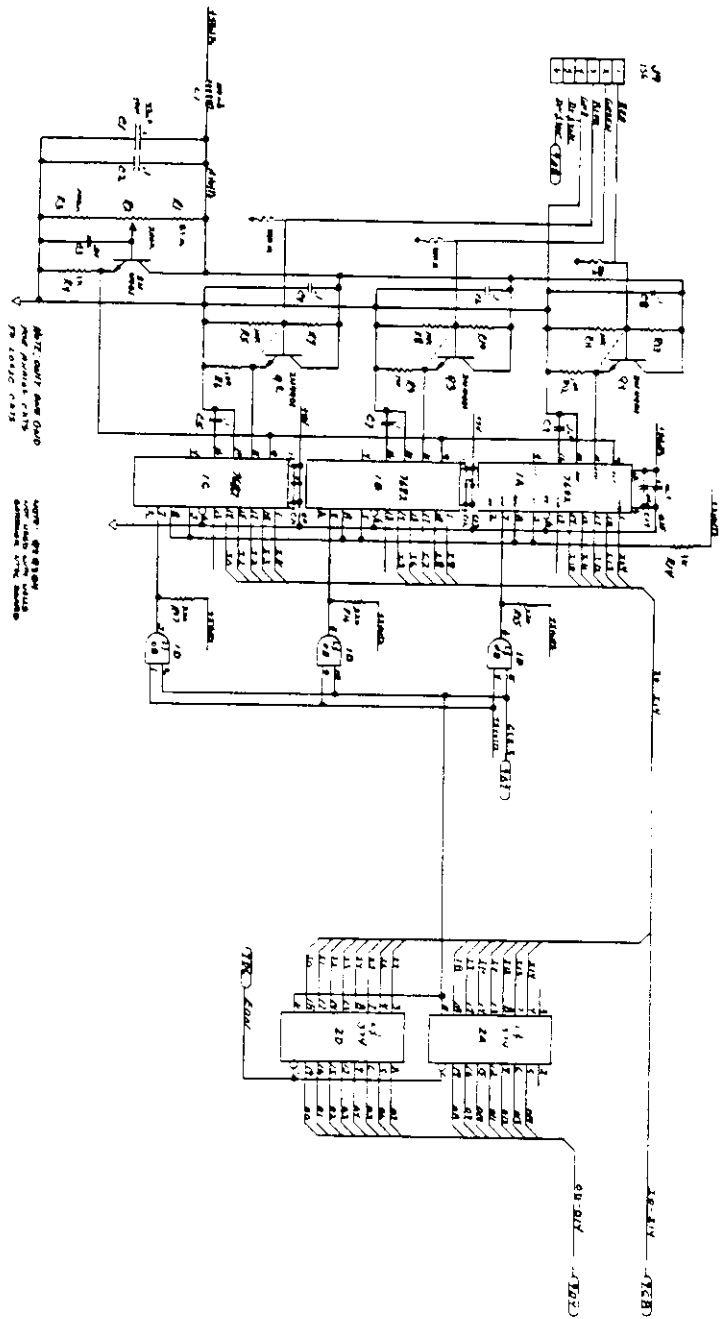
The Expander functions to store a line of video which has been converted to digital by the analog to digital converter, on page 10. This digital data is in a form of 5 bits per color (5 for each red, green and blue) for a total of 15 bits of data. This data is applied to an odd and even line buffer RAM system (B5,B4,B3,B2 and C5,C4,C3,C2) through buffer registers (A3,D3 and A4,D4). The data is stored sequentially by counters (B8,B7,B6 and C8,C7,C6) in the buffer RAMs at a 12mhz rate. At the start of each display line data stored in the buffer RAM during the previous line is available to be displayed during the current line. The address of the start location in the buffer RAM originates from the main logic pcb and is used to define the start position of the expanded line. When the data is read from the buffer RAM, it is read at a 6mhz rate which appears on the screen display as a normal line of data, only shifted in the left or right direction.



## A TO D CONVERTER EXPANDER SCHEMATIC PAGE 10 of 10

Schematic Grid Location	Board Location	Function
D7,C7	Q4,Q3,Q2	RGB analog video input buffers
B7	Q1	Analog voltage range control
D6,C6	A1,B1,C1	RGB analog to digital converters
C4	A2,D2	Expander bypass buffers

The input through P9 is from the NTSC to RGB converter pcb. This input is an analog voltage for the three colors: red, green, and blue. Each analog color voltage is converted to digital data by separate analog to digital converters (A1,B1,C1). The output of these converters form a 15 bit word that is made up of 5 bits of color for each red, green, and blue. This data word is then applied to the odd/even line buffers or directly to the output of the expander. The adjustment of R2 allows the dynamic range of the analog to digital converter to be set. This adjustment interacts with the contrast control on the NTSC converter board.



NOTE: THIS CIRCUIT IS FOR THE ATOD CONVERTER EXPANSION. IT IS NOT TO BE USED FOR THE ATOD CONVERTER.

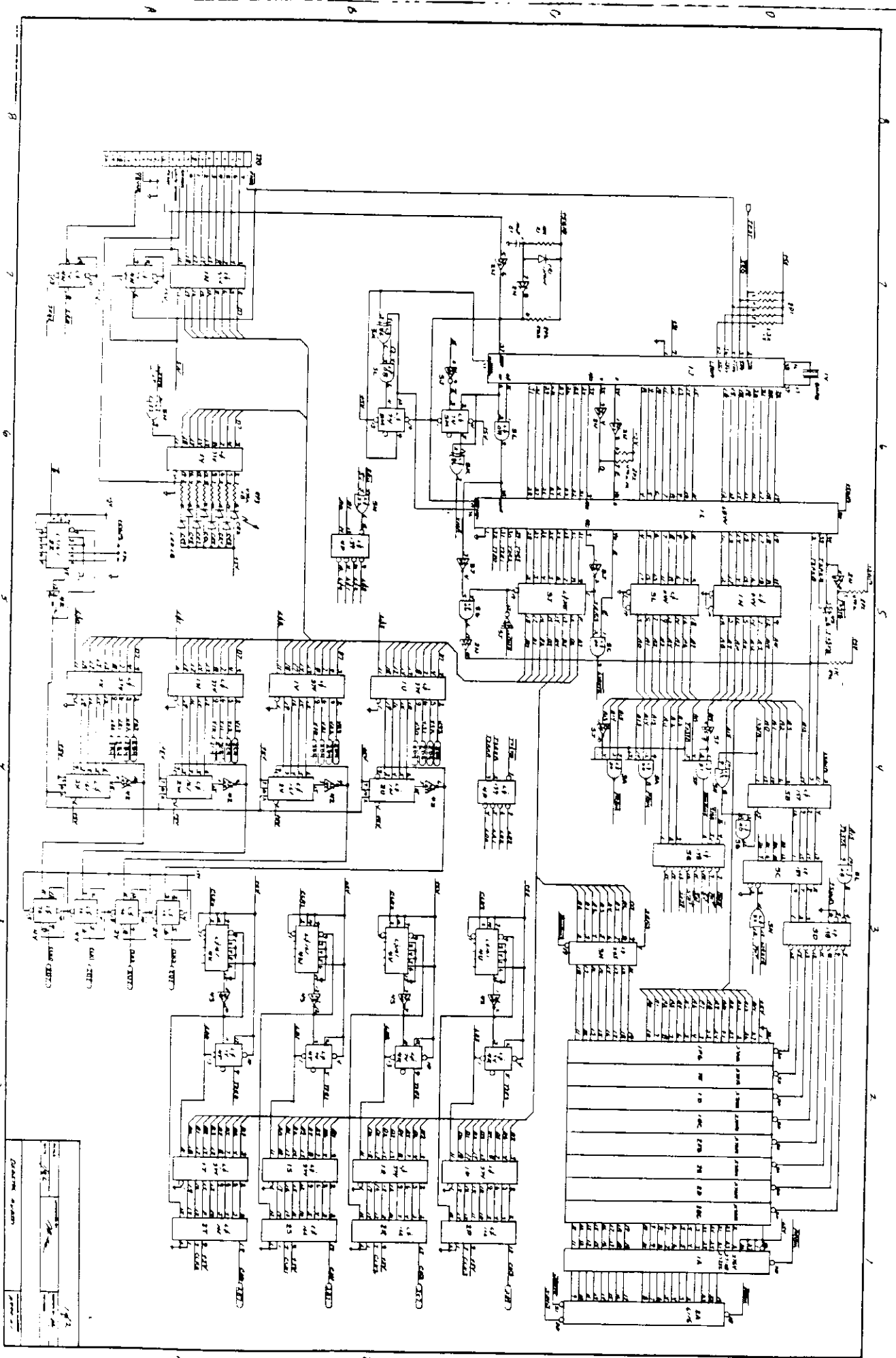
8	7	6	5	4	3	2	1
PROJECT NO. DATE DRAWN BY CHECKED BY APPROVED BY TITLE D ATOD CONVERTER EXPANSION		PART NO. QUANTITY UNIT 10 10		REV. DATE BY 1/10 10		PART NO. QUANTITY UNIT 10 10	

## DIGITAL AUDIO SCHEMATIC PAGE 1 of 2

Schematic Grid Location	Board Location	Function
D7	J1	Audio system CPU
C7	N2	Power on reset circuit
A7	N1	Audio board command input buff
A6	Y1	Audio system status reg
A5	Z2	Low speed clock generator
D6	L1	DMA device
B6	M5	DMA grant and control
B5	P4	Address decode 1 of 4 channels
D5	1H,3L	Address line buffers
C5	3J	Data line buffer
D4	B5	DMA or CPU to ROM control
D3	C5	Bank address control RAM
D3	D5	ROM enable decoding
D3	E2	CPU address decoding
D4	A5	CPU ROM or RAM decoding
C3	H3	ROM and RAM data buss buffer
D2	F1,E1,D1,B1,F2,E2,D2,B2	Digital Audio data ROMs
D1	A1	Audio CPU program ROM
D1	A2	Audio CPU system RAM
B4,A4	U1,V1,W1,X1	Clock rate and volume control
B4,A4	U2,V2,W2,X2	Channel clock rate generator
A3	Y2,Y4	Channel clock rate buffers
B3	U4,V4,W4,X4	Channel reload control
B2	R4,T4	Channel reload flag flip flop
B2	P1,R1,S1,T1	Channel data buffer
B1	P2,R2,S2,T2	Channel parallel to serial

The heart of the digital audio system is a MC6809 central processing unit (J1) and the MC6844 DMA device (L1). The program data is stored in the ROM located at (A1), and the digital audio data is stored in ROMs at locations F1, E1, D1, B1, F2, E2, D2, and B2. This stored data is accessed by the DMA device, and then transferred to one of the four audio channels. Control of the DMA device is performed by the CPU, which sets up addresses and count data.

Each audio channel has a controllable clock rate for the conversion of parallel data to serial data. This clock rate determines the rate at which data is applied to the delta demodulator devices, located on page 2 of the audio logic diagram.



TABLE

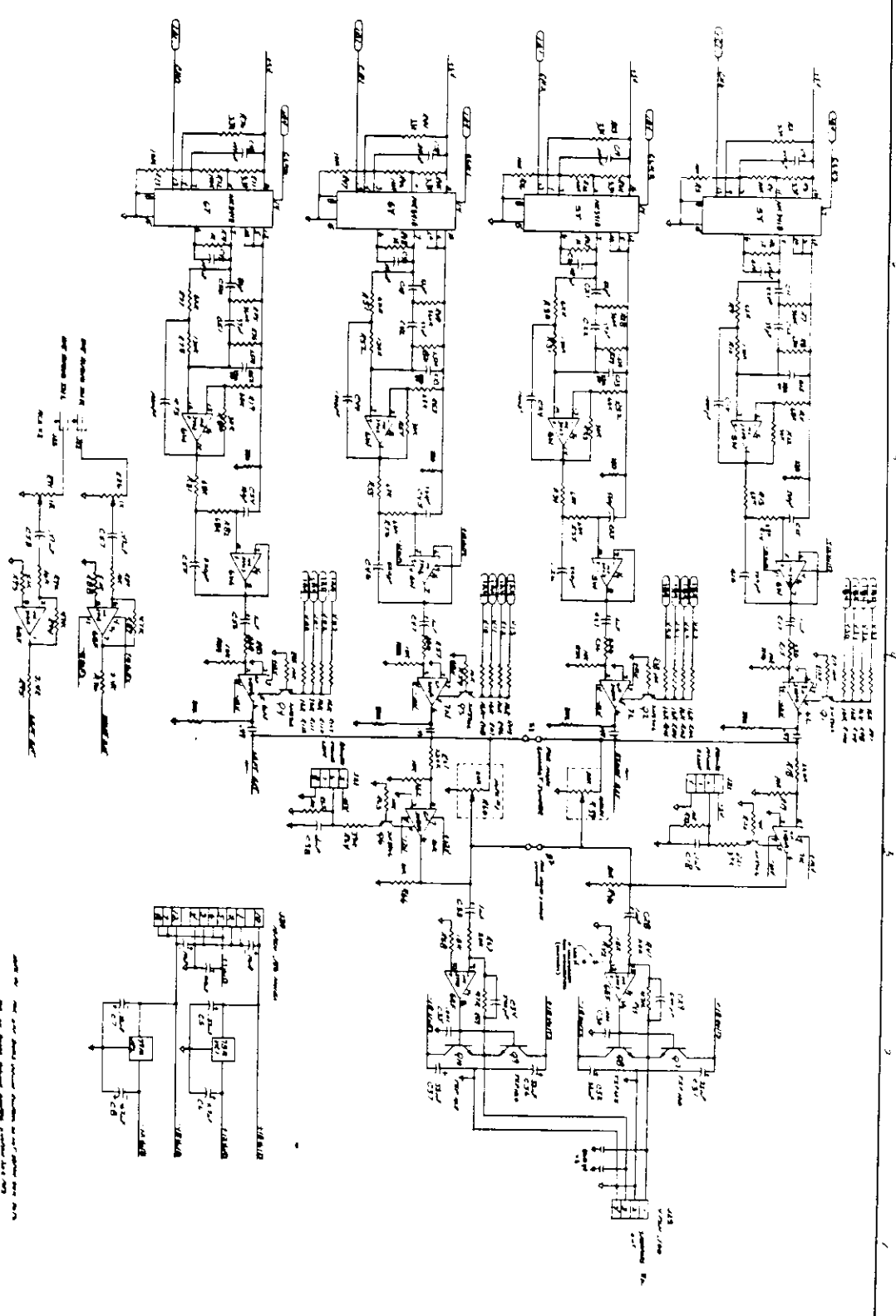
NO.	DESCRIPTION
1	RELAY R1
2	RELAY R2
3	RELAY R3
4	RELAY R4
5	RELAY R5
6	RELAY R6
7	RELAY R7
8	RELAY R8
9	RELAY R9
10	RELAY R10
11	CONTACTOR C1
12	CONTACTOR C2
13	CONTACTOR C3
14	CONTACTOR C4
15	CONTACTOR C5



## ANALOG AUDIO SCHEMATIC PAGE 2 of 2

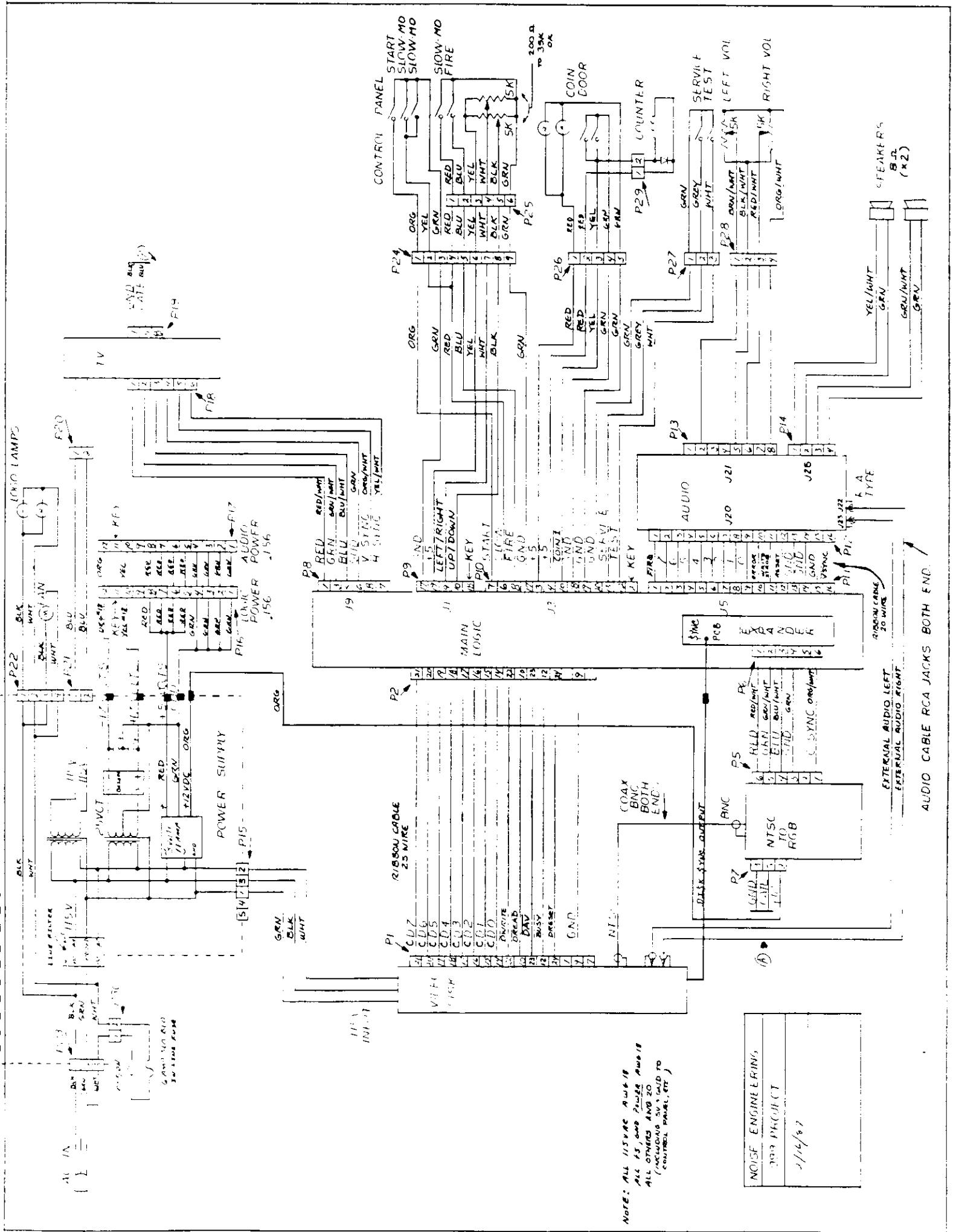
Schematic Grid Location	Board Location	Function
D6,C6,B6	Y5,T5,Y6,T6	Serial digital to analog
D5,C5,B5	W5,W6	Channel low pass filters
D4,C4,B4	L6,L7,N7,N6	Channel volume control
D3,C3	K7,K6 (Opt.)	External volume control
D2,C2	E6	Power amplifier drivers
D2,C2	Q7,Q8,Q9,Q10	Power amplifier output drivers
A4	E6	External audio input buffers
B2	VR1,VR2	Audio power regulators

The conversion from serial digital data to analog data is accomplished by the MC3418 devices (Y5,T5,Y6,T6). Then the analog data is sent through a low pass filter circuit, MC3403s (W5,W6) to remove conversion noise. The amplitude of the analog signals are then controlled by the electronic attenuators CA3080 (L6,L7,N7,N6). External left and right audio from the video disk player is applied through amplifier buffers MC3403s (E6). This audio is combined with the digital generated audio output of the CA3080 and both are applied to the dual audio power amplifiers. The dual audio power amplifiers are made up of the MC3403 (E6) amplifier driver and transistors (Q7,Q8,Q9,Q10).



NOTE: The use of standard values for components not shown is permitted. The use of standard values for components not shown is permitted. The use of standard values for components not shown is permitted.

DATE	2/7/73
DESIGNED BY	
CHECKED BY	
APPROVED BY	
PROJECT NO.	907070



NOTE: ALL 115VAC AWG 18  
 ALL 25, 30W POWER AWG 18  
 ALL OTHERS AWG 20  
 (INCLUDING 5V GND TO  
 CONTROL PANEL, ETC.)

NOISE ENGINEERING
300 PROJECT
1/16/67

AUDIO CABLE RCA JACKS BOTH END.

EXTERNAL AUDIO LEFT  
 EXTERNAL AUDIO RIGHT

20 WIRE

TYPE

J26

J20

J21

AUDIO

P27

P28

P29

COUNTER

COIN

DOOR

P26

P25

P24

CONTROL PANEL

START

SLOW MO

SLOW MO

FIRE

200 Ω

35K Ω

5K Ω

5K Ω

5K Ω

5K Ω

5K Ω

5K Ω

5K Ω

5K Ω

5K Ω